# Visualization, modeling and control of filament growth in resistive-memories (RRAMs) towards commercial applications

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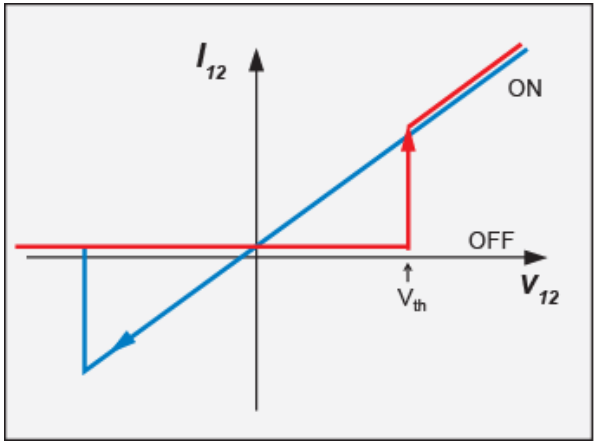
IEEE Nano, July 28, 2015

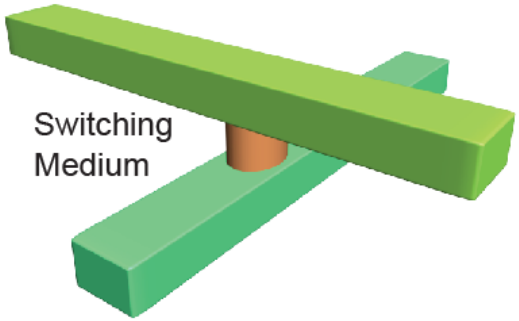
# Introduction: Resistive Switching Devices

## Hysteretic resistive switches and crossbar structures

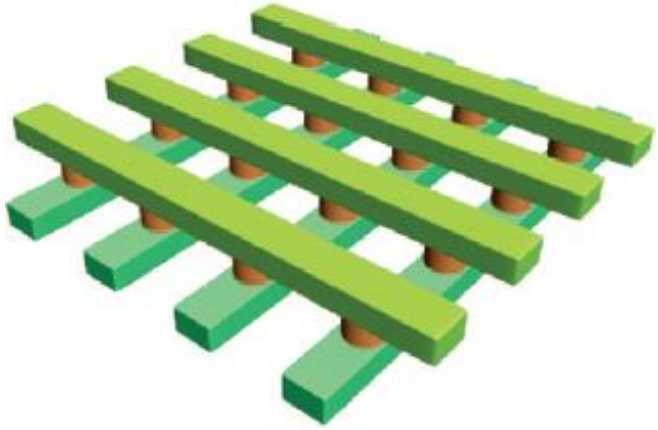
- Simple structure
  - Formed by two-terminal devices
  - Not limited by transistor scaling
- Ultra-high density
  - NAND-like layout, cell size $4F^2$
  - Terabit potential
- Large connectivity
- Memory, logic/neuromorphic applications




### Single-cell structure

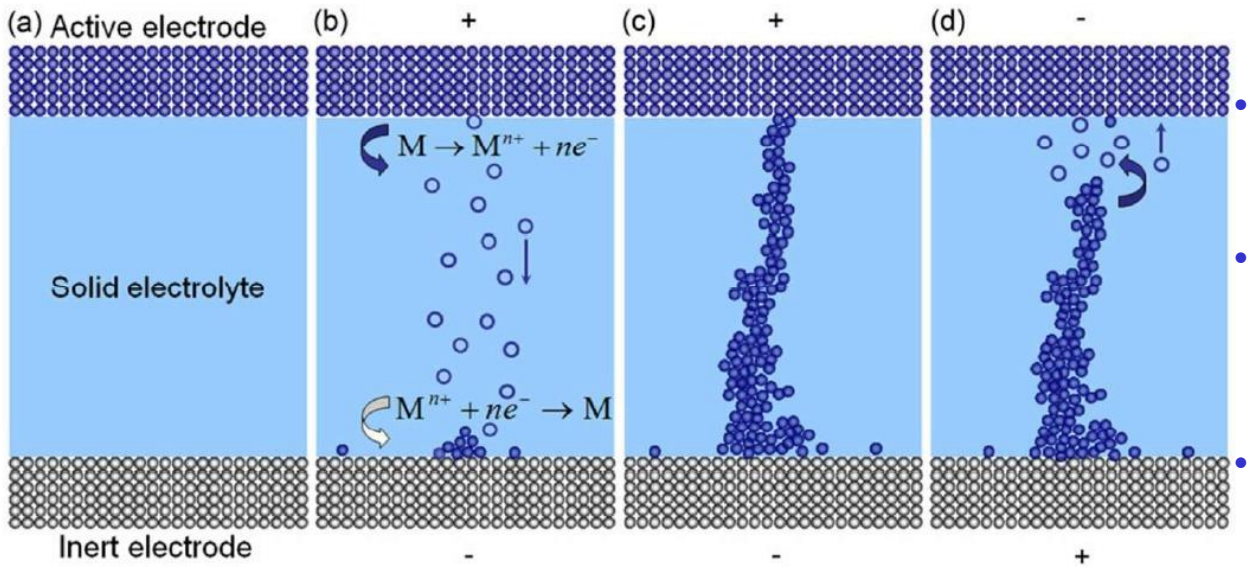



### Crossbar Structure



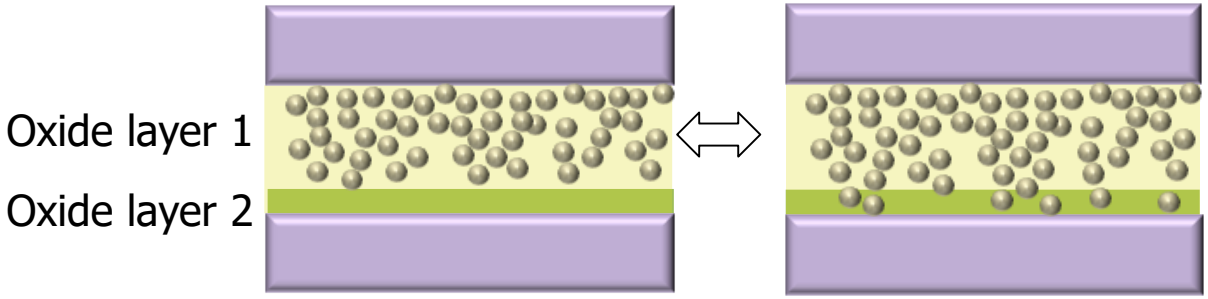
# Electronics Based on Ions: Resistive Memory

## ElectroChemical Metallization Cell (ECM, CBRAM)




- *Creating "new" materials on the fly*
- Active electrode material + inert dielectric
- "Filament" based on electrode material injection and redox at electrodes
- Switching layer facilitates ionic movement

## Valency Change Cell (VCM)




- *Modulating exiting material properties*
- Filament based on oxygen exchange between two oxide layers
- Electrode plays minor role

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*Yuchao Yang and Wei Lu, Nanoscale*, 5, 10076 (2013)

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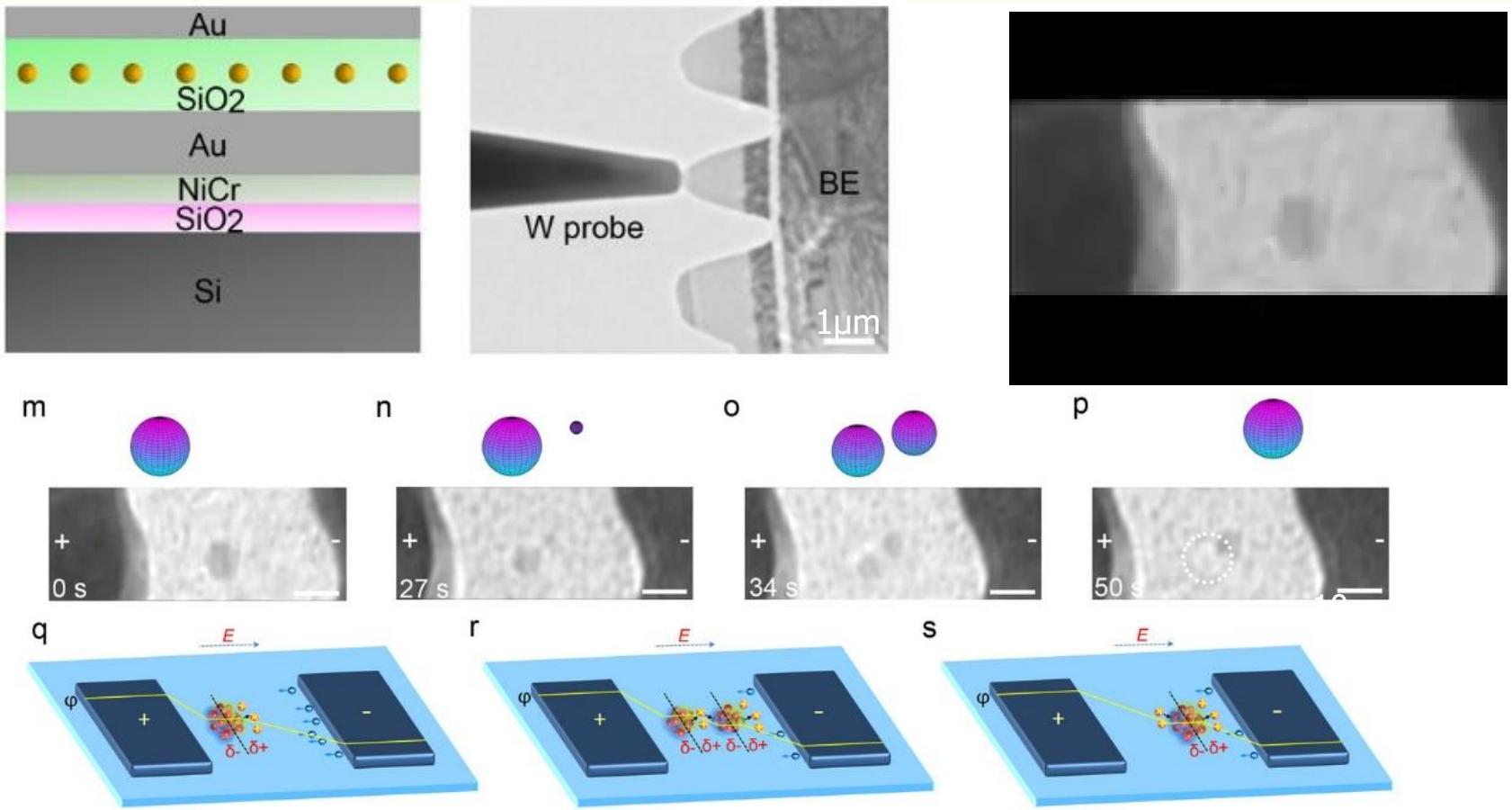
# Microscopic Origin of Dynamic Particle Migration




- Particles form bipolar electrodes, with redox processes happening at opposite sides
- Dissolution of the original Ag particle leads to new particle nucleation and growth at downstream position
- Resulting in effective Ag particle migration in the electric field direction

Y. Yang, Gao, Li, Pan, Tappertzhofen, Choi, Waser, Valov, W. Lu, Nat. Comms. 5, 4232 , 2014

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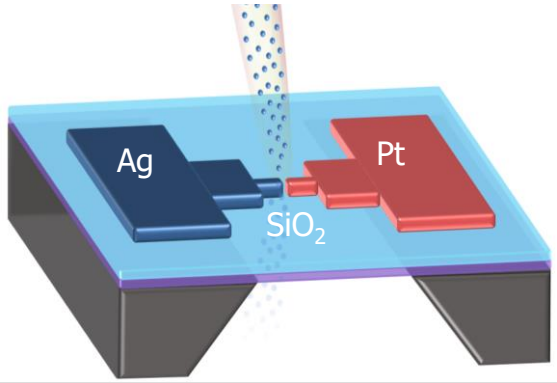
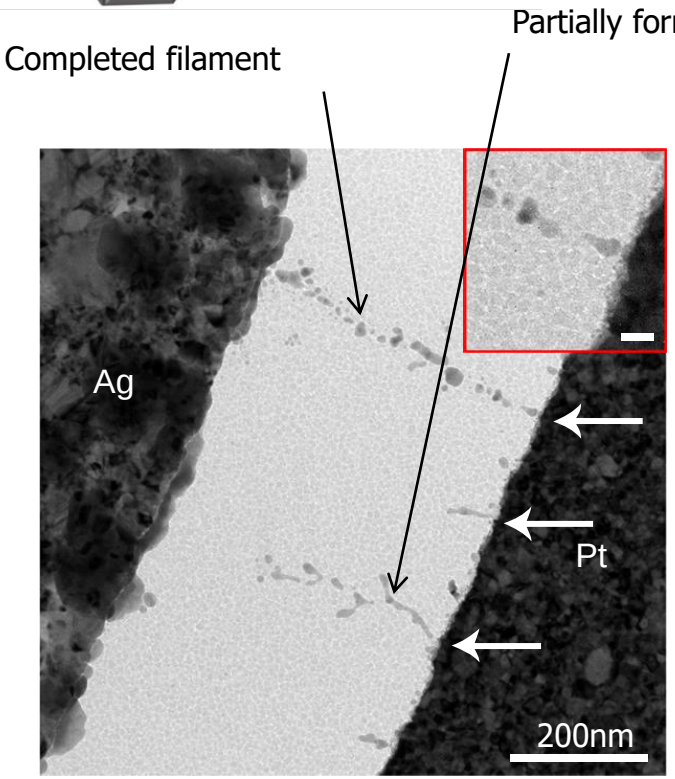
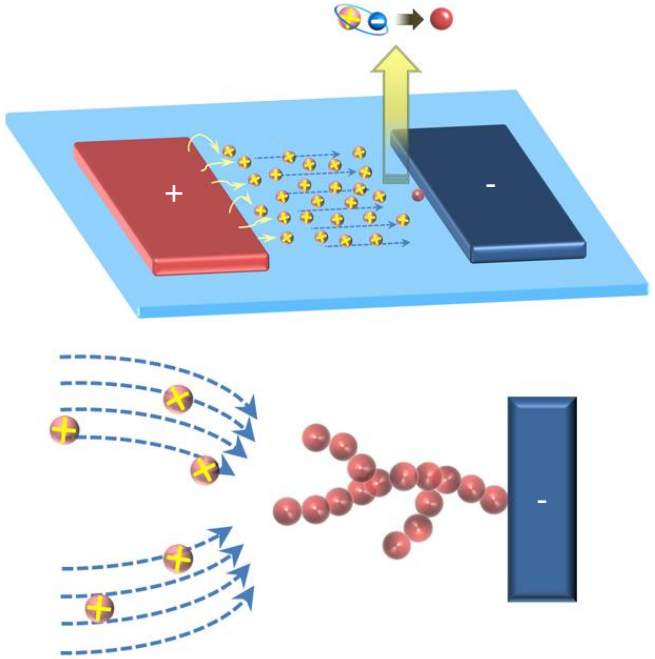
# Visualization of Filament

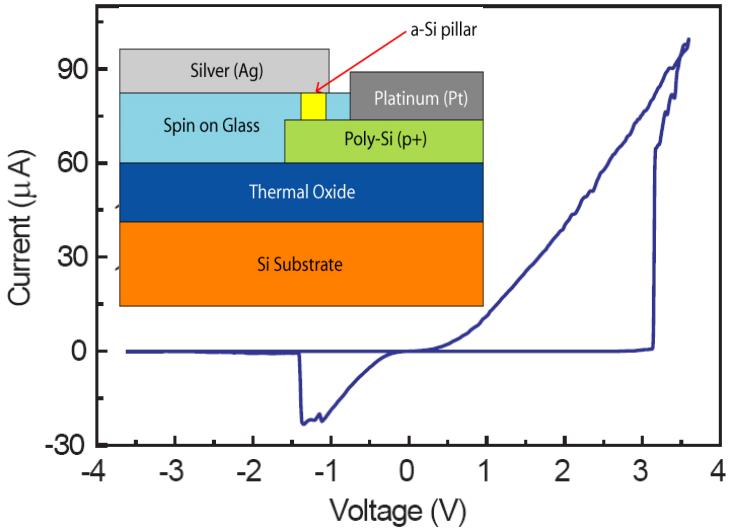


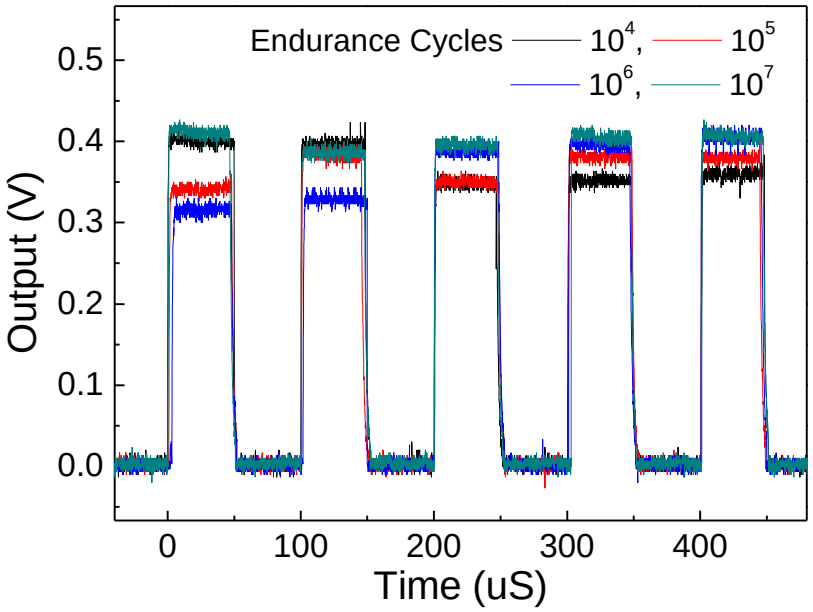

- **Ag/$SiO_2$/Pt structure, sputtered $SiO_2$ film**
- **The filament grows from the IE backwards toward the AE**
- **Branched structures were observed with wider branches pointing to the AE**

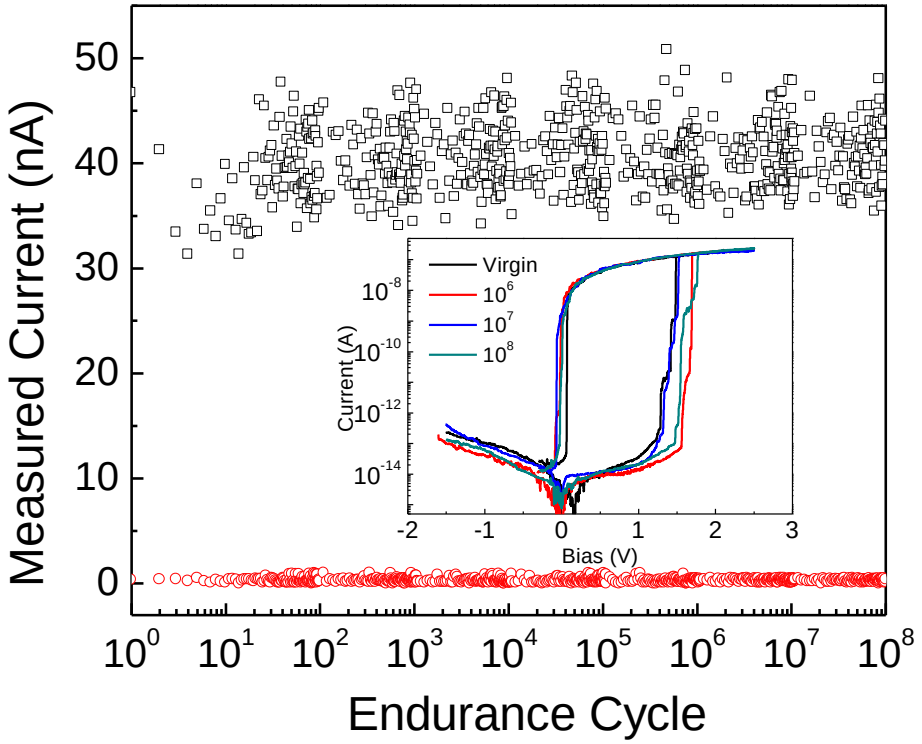


# Resistance Switching Characteristics



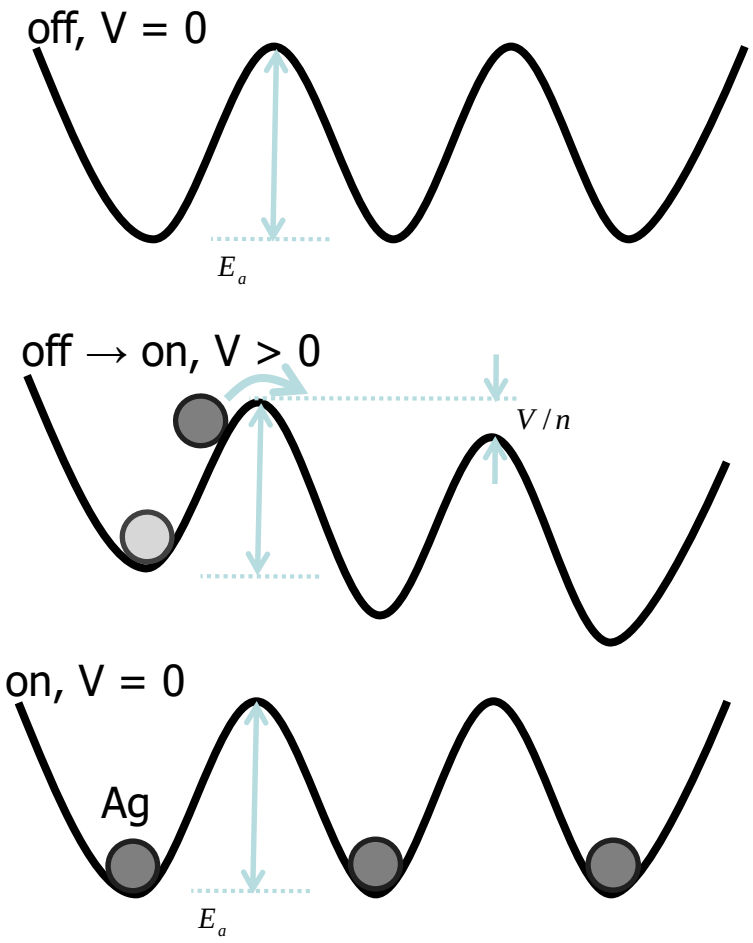




- **1e6 on/off**
- **1e8 W/E endurance**
- **Switching speed ~10ns**


**Jo, Kim, W. Lu, *Nano Lett.*, 8, 392 (2008)**

**Kim, Jo, W. Lu, *Appl. Phys. Lett.* 96, 053106 (2010)**

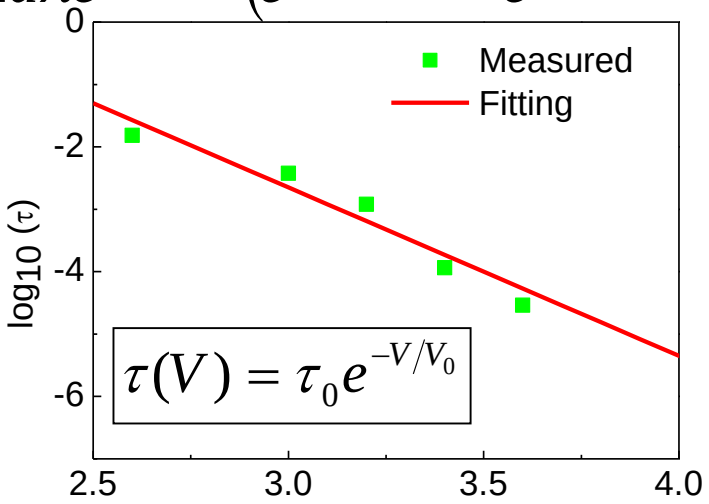
# Driving Ions with Electric Field

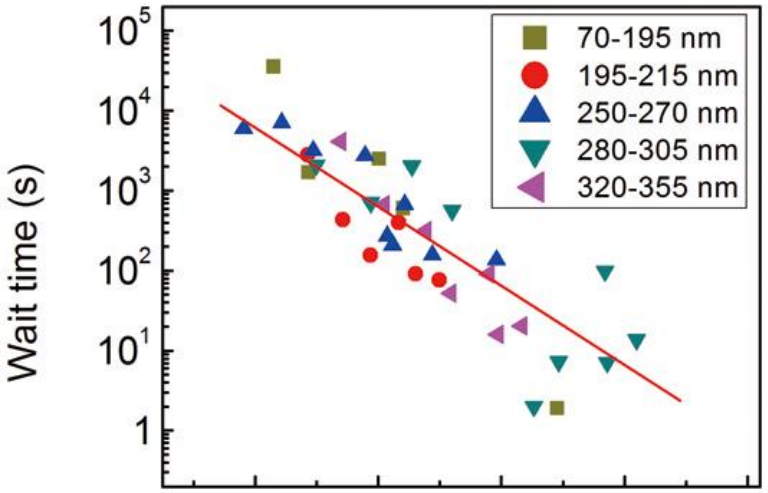



$$\Gamma = 1/\tau = \upsilon e^{-E_a'(V)/k_BT}$$

$$E_a'(V) = E_a - V/2n$$

$$v = 2d\lambda e^{-E_a/k_BT}\left(e^{qEd/2k_BT} - e^{-qEd/2k_BT}\right)$$

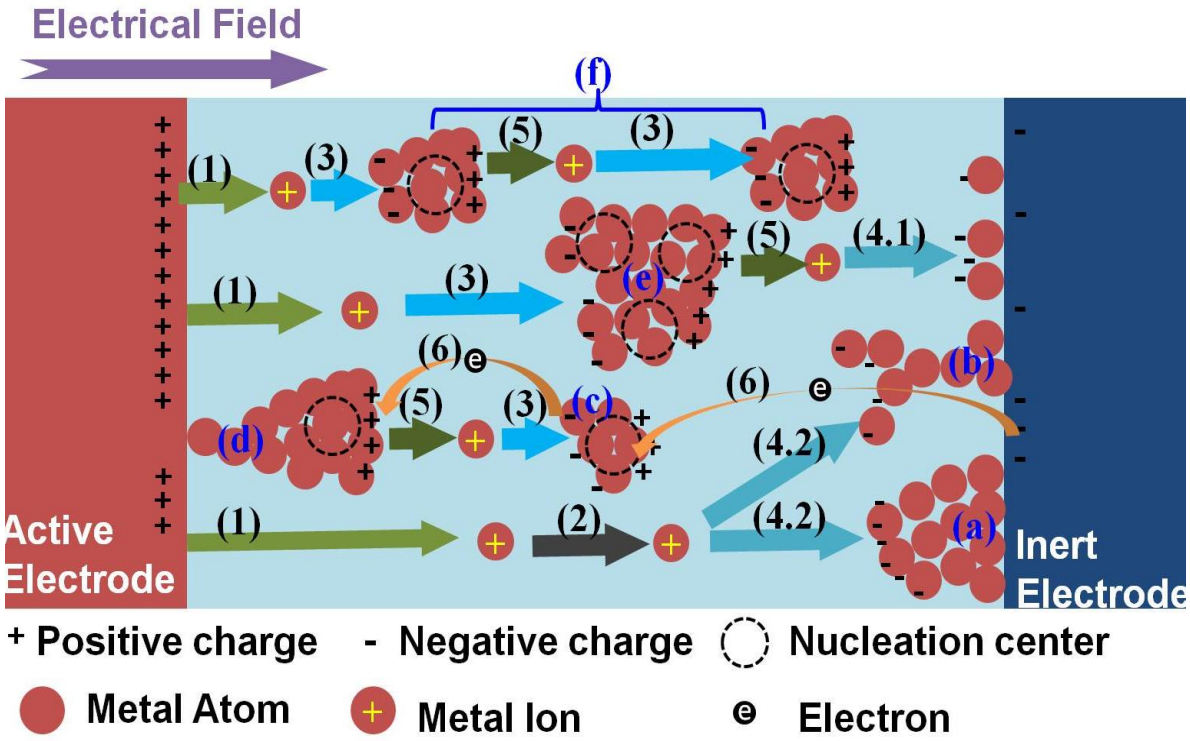



- Filament formation is a thermally activated process.
- Activation energy reduced by applied bias.
- Speed is a ca. *exponential* function of voltage.

**Jo, Kim, Lu *Nano Lett.* 9, 496-500 (2009).**

# Dynamic Monte Carlo Simulation



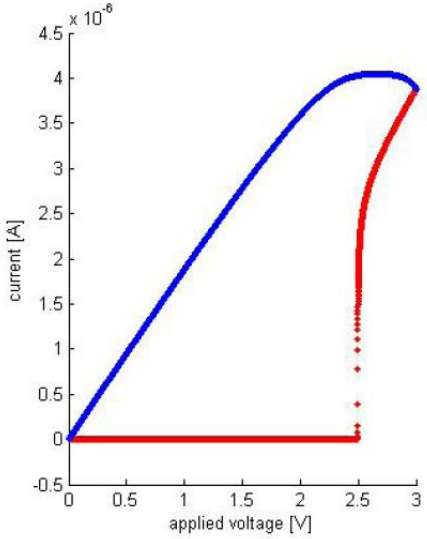

**Observed phenomenon in ECM**

**(a) Me atoms accumulated near IE**
**(b) Branched filament formed**
**(c) Me nuclei formed in dielectrics**
**(d) Me nuclei reconnected with AE**
**(e) Me nuclei agglomerate**
**(f) Me nuclei transport in dielectrics**
*** Metal atoms nuclei (AN)**

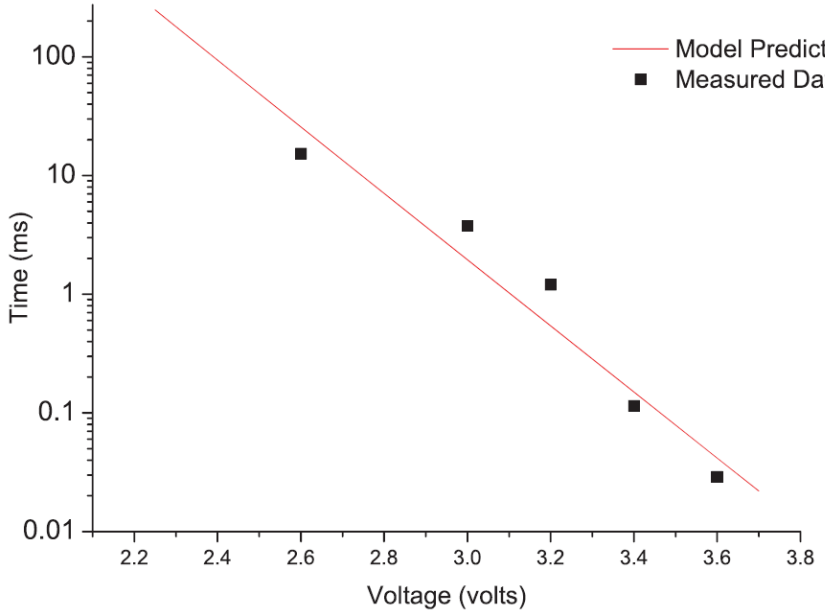
**Microscopic physical processes during SET**

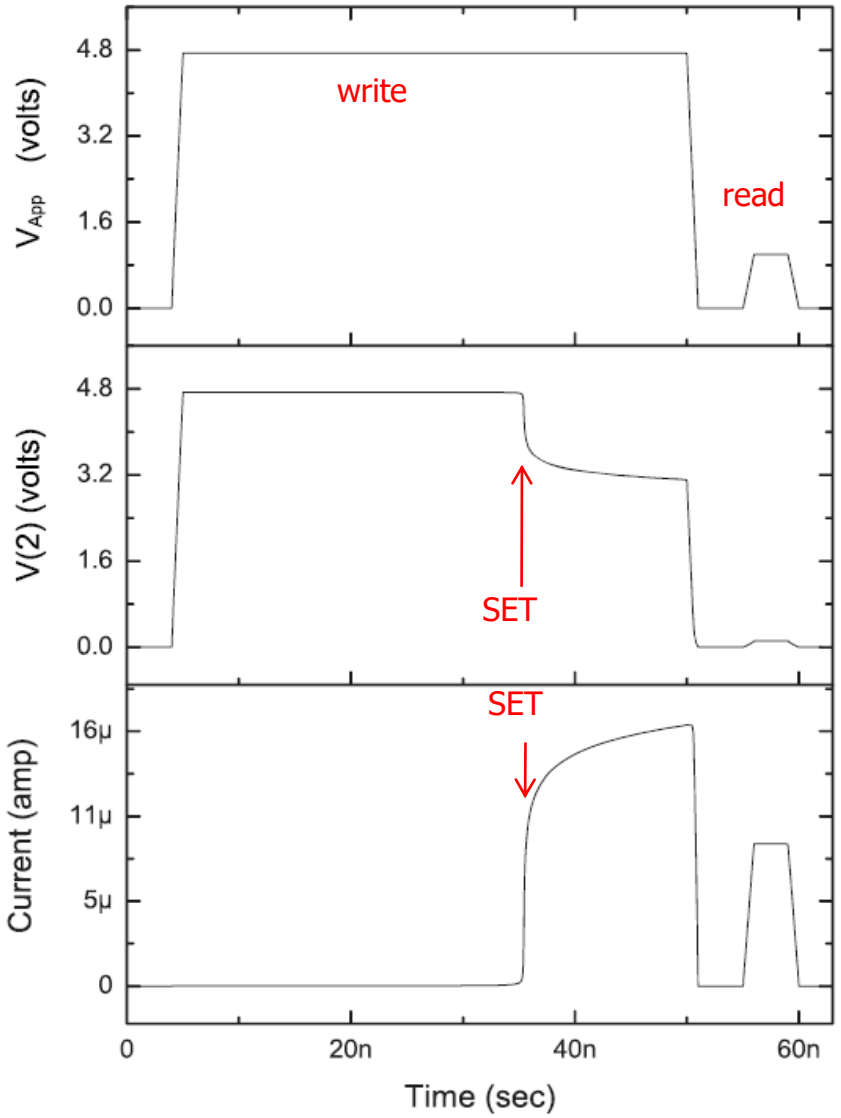
**(1) Ionization of metal atoms in AE (anodic dissolution)**
**(2) Metal ions hopping in dielectrics**
**(3) Metal ions attachment to existing clusters**
**(4) Nucleation of metal ions captured by (4.1) IE and (4.2)**
**(5) Metal atoms in nuclei are activated to ions**
**(6) Electron hopping from IE to Neutralize positive charge from metal ions**

# SPICE Model



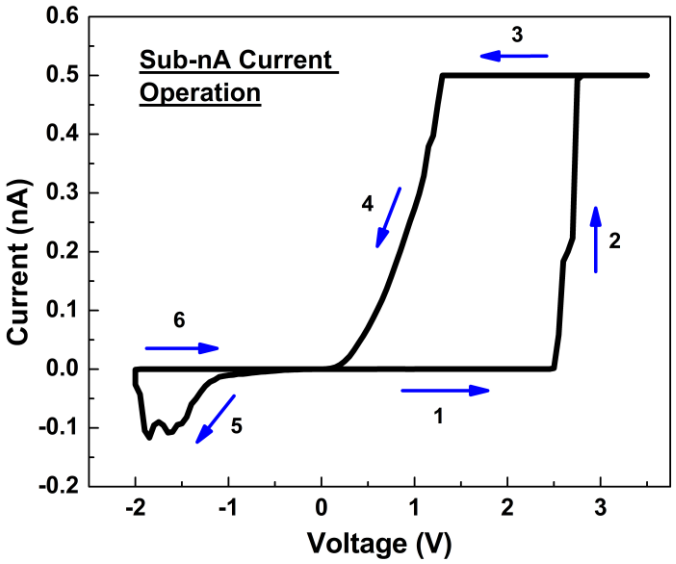

- **RRAM switching transient effects captured in SPICE**

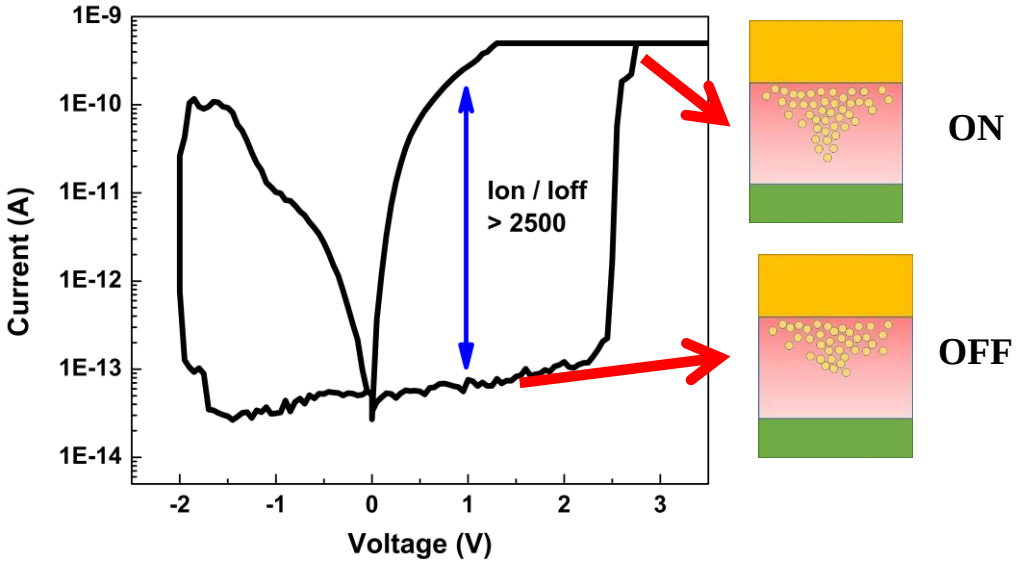



Sheridan, Kim, Lu, *Nanoscale* 3, 3833 (2011).

# CBRAM - Sub-1nA On-Current



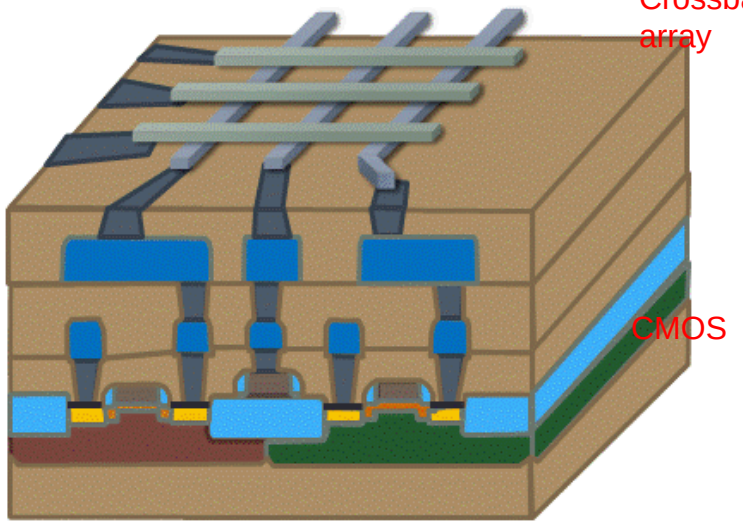

- Precise control of the filament shape during set.
- Controlled and stable tunneling gap may be maintained.

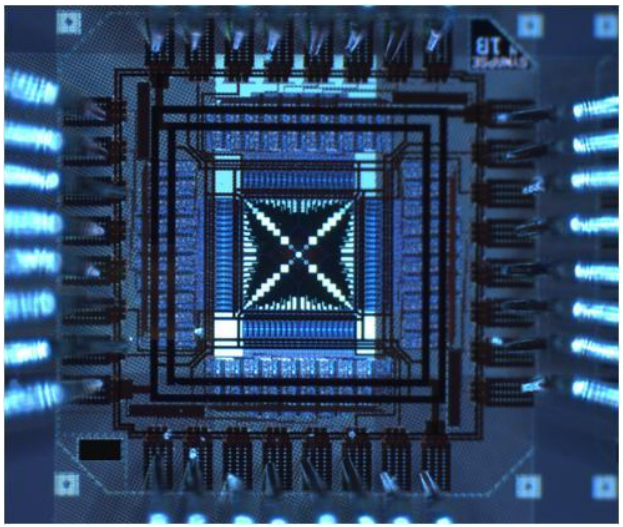
**Compared with oxide-RRAM, CBRAM offers**

- Higher on/off ratio due to very low $I_{off}$
- Lower $I_{on}$ and better variability

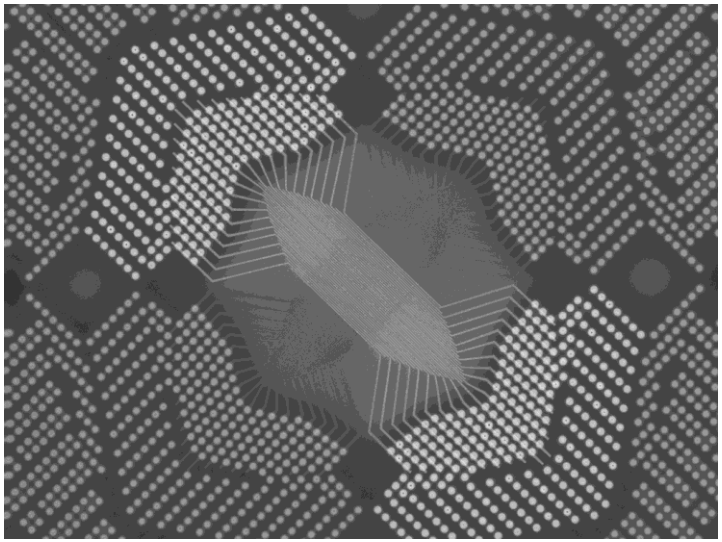
S. Gaba, F. Cai, J. Zhou, and W. Lu, *IEEE Elec. Dev. Lett.* 35, 1239 - 1241, 2014

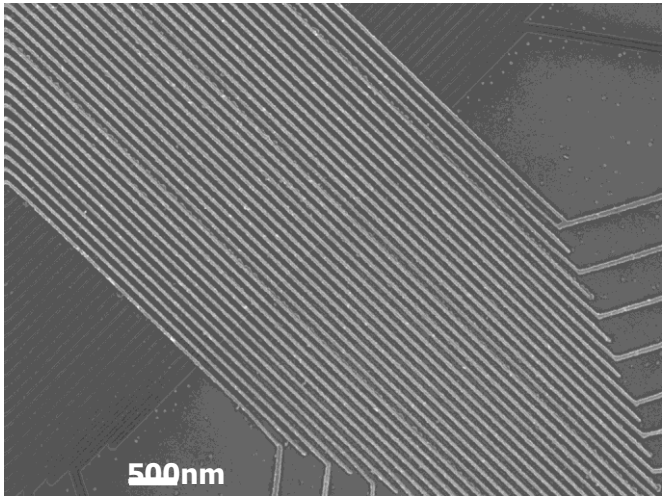
# Integrated Crossbar Array/CMOS System



- Low-temperature process, RRAM array fabricated on top of CMOS
- CMOS provides address mux/demux
- RRAM array: 100nm pitch, 50nm linewidth with density of 10Gbits/cm$^2$
- CMOS units – larger but fewer units needed. 2n CMOS cells control n$^2$ memory cells



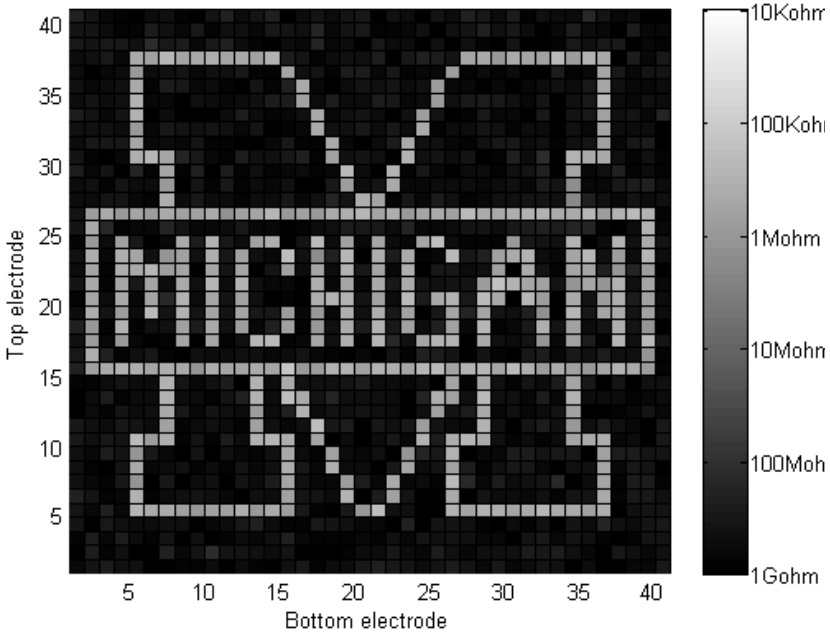



Kim, Gaba, Wheeler, Cruz-Albrecht, Srivinara, W. Lu *Nano Lett.*, 12, 389–395 (2012).

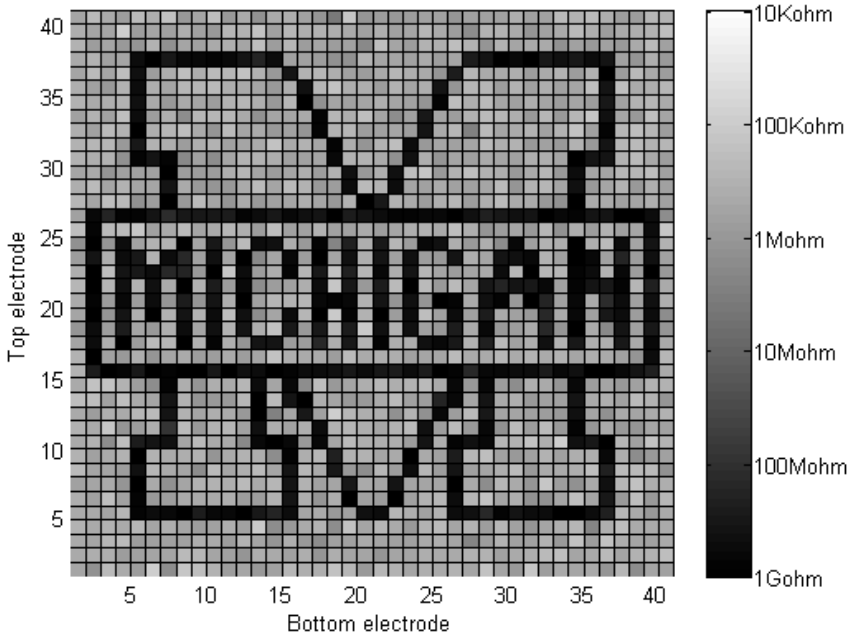
# Integrated Crossbar Array/CMOS System

- **Crossbar array operation, array written followed by read**
- **Programming and reading through integrated CMOS address decoders**
- **Each bit written with a single pulse**

Stored/retrieved array 1




Stored/retrieved array 2




**Results from a 40x40 crossbar array integrated on CMOS**

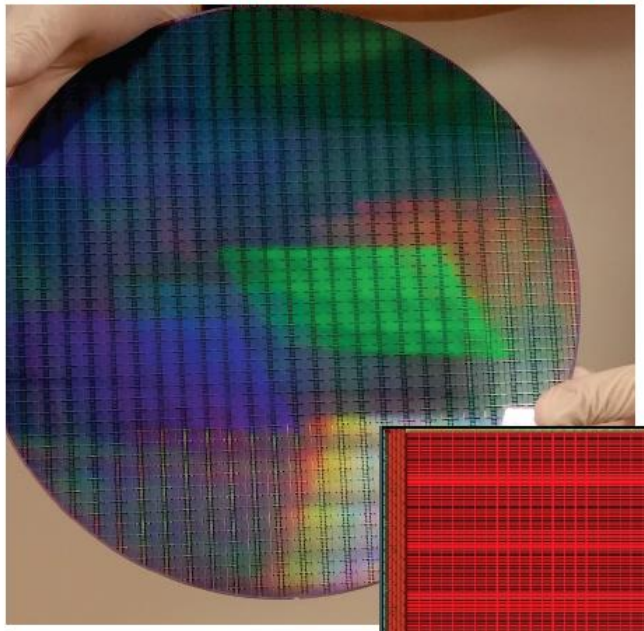
**Kim, Gaba, Wheeler, Cruz-Albrecht, Srivinara, W. Lu *Nano Lett.*, 12, 389–395 (2012).**

# From Lab to Fab: Crossbar RRAM Technology

- **CMOS** Compatible
- **3D** Stackable, Scalable Architecture – Low thermal budget process
- **Architectures** proven include multiple Via schemes and Subtractive etching
- **Crossbar Inc** founded in 2010, received over $85M Venture Capital funding to date.

Complete

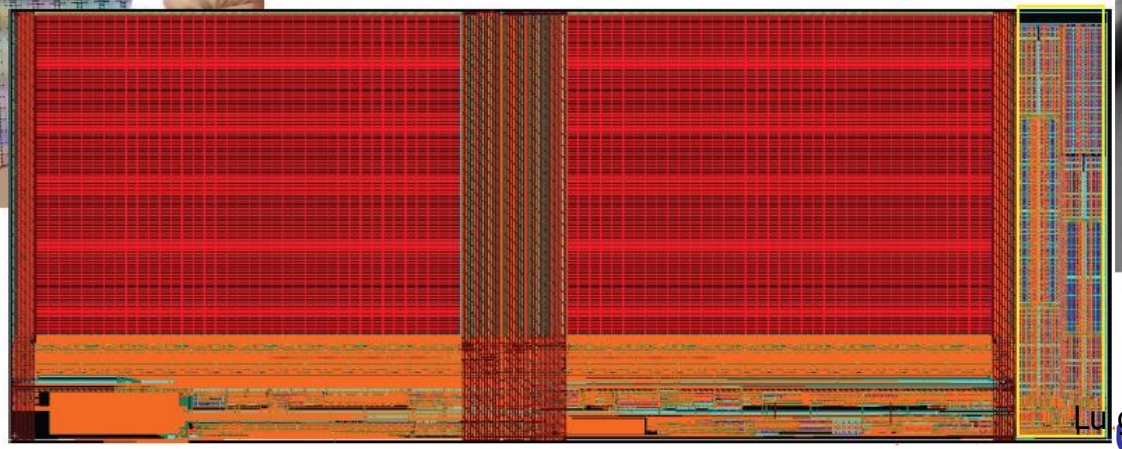
Crossbar RRAM 300mm wafer



Crossbar

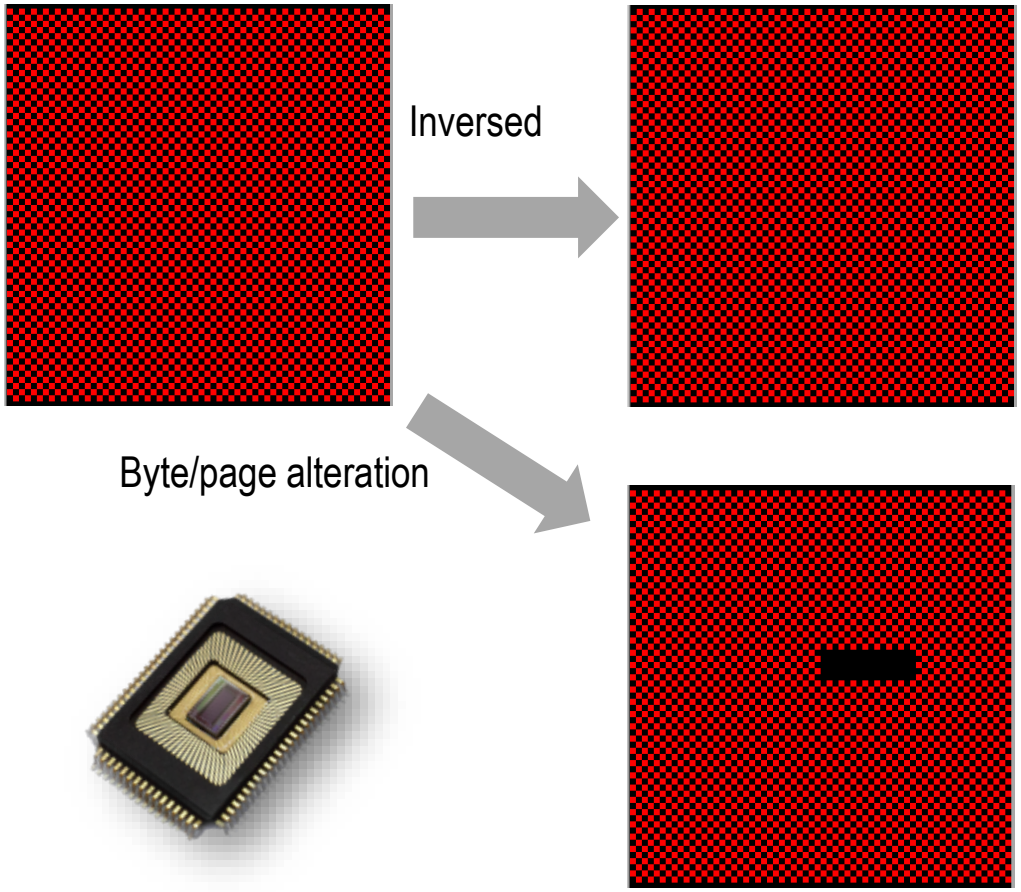
**July 2015**

Crossbar Embedded RRAM (1T1R)



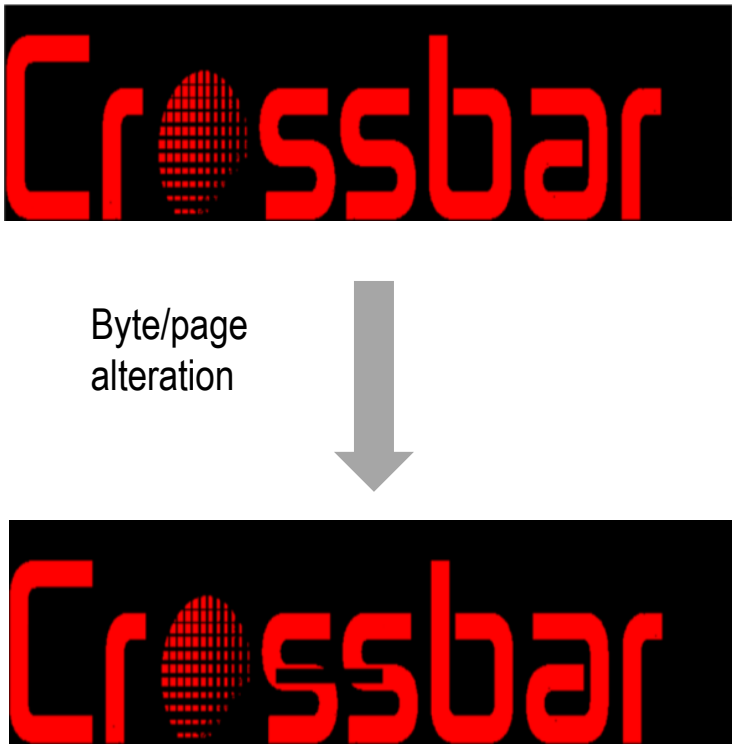
# Mb 1T1R CBRAM Chips

## Checkerboard pattern





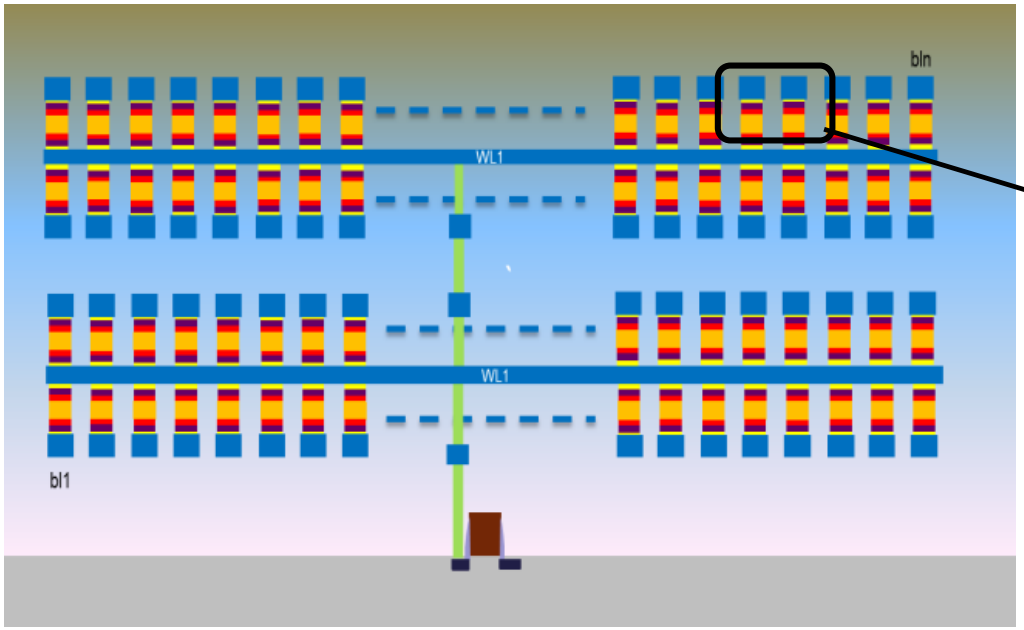

## Random pattern



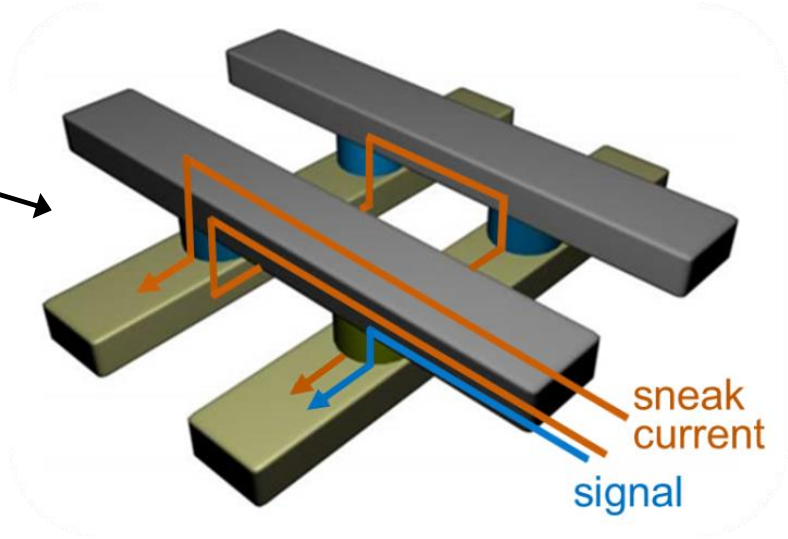
# Challenge in 1TnR – Sneak Current

- Cross-point array architecture for 1TnR implementation
- Multiple sneak (leakage) current paths exist
  - Limited array size
  - Diminishing read margin and increased power consumption

**1TnR architecture**

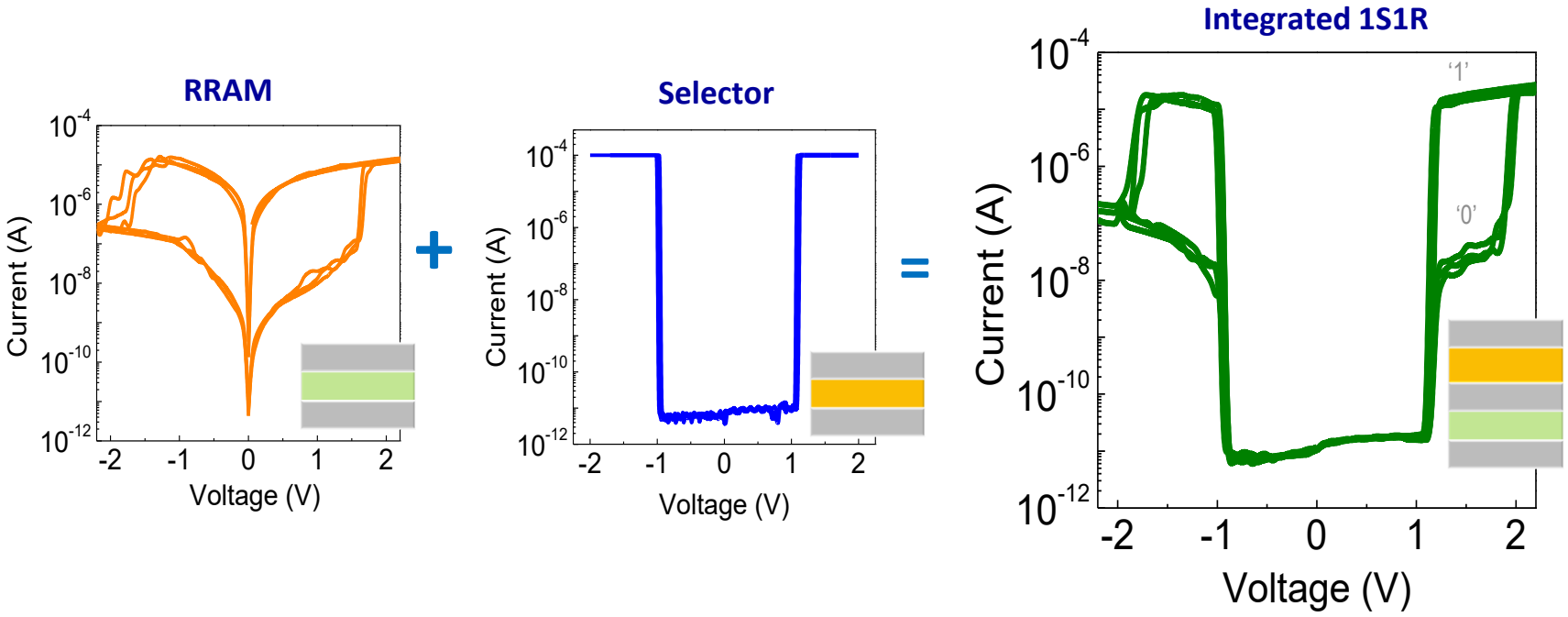



**Cross-point structure**



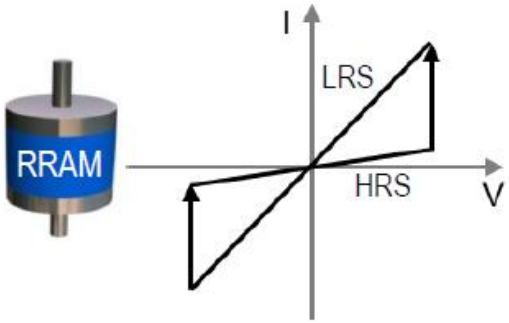
# RRAM + Selector (1S1R)

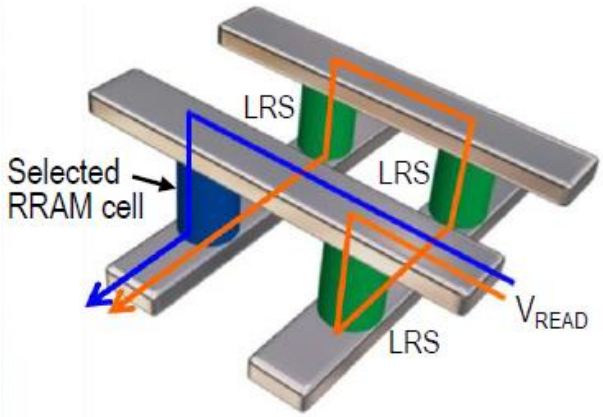
- Cross-point array integration of RRAM + Selector
  - High HSR & sharp switching slope of a selector
  - Small voltage overhead for selector integration



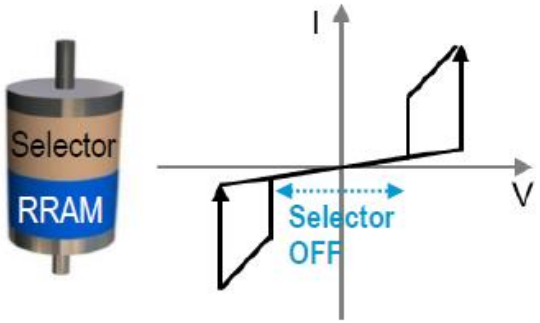
# IS1R Structure

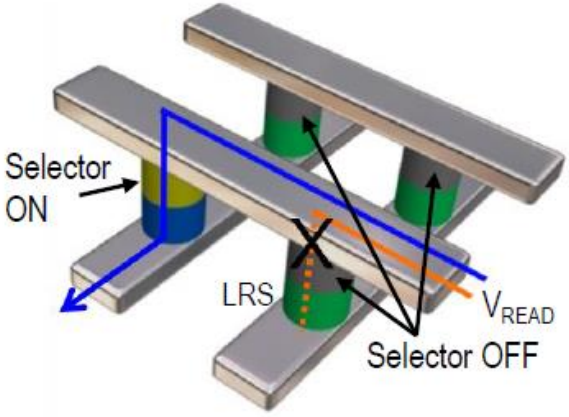
Cross-point array with linear RRAM only



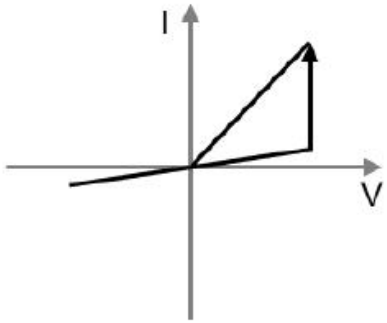



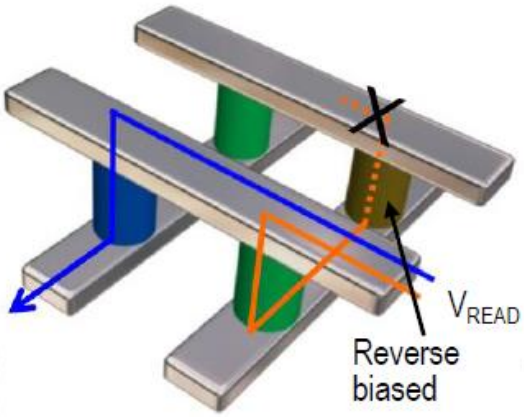

Cross-point array with RRAM + selector




Cross-point array with rectifying RRAM or unipolar RRAM w/ a diode




Sensing current from a selected cell

Leakage current

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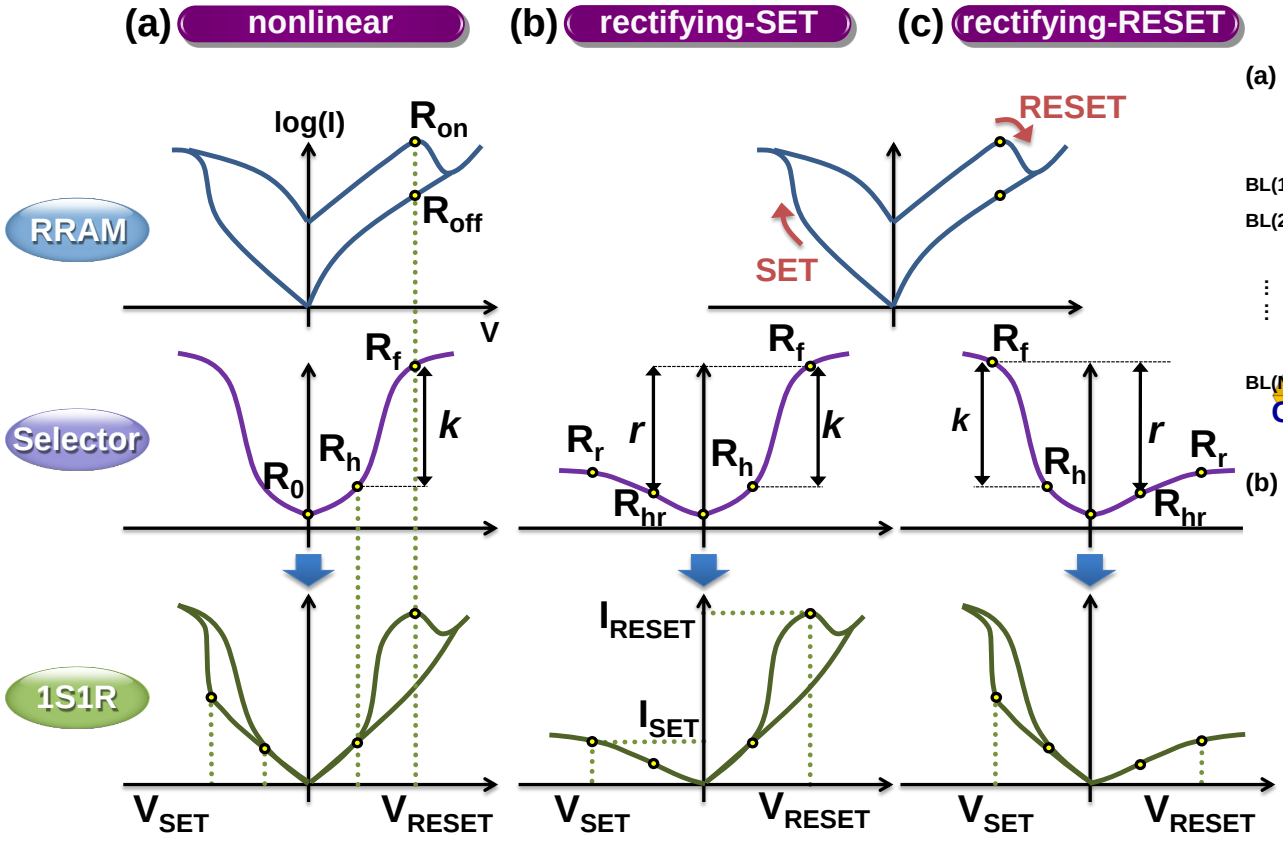
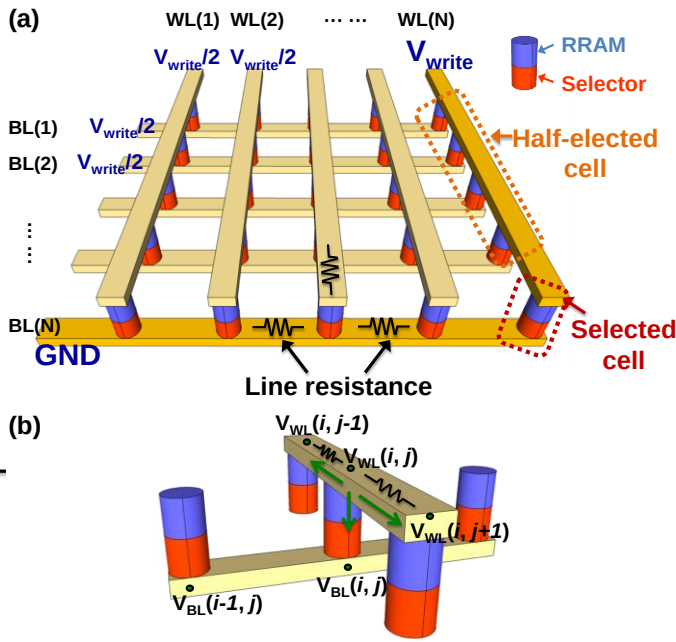
# Selector Analysis During Write




Kim et al. IEEE TED, 61 (8), 2820-2826 (2014).

- V/2 bias scheme as example
- Rectifying behavior alone does not help
- Non-linear effect is necessary
- Current density and sub-threshold slope critical

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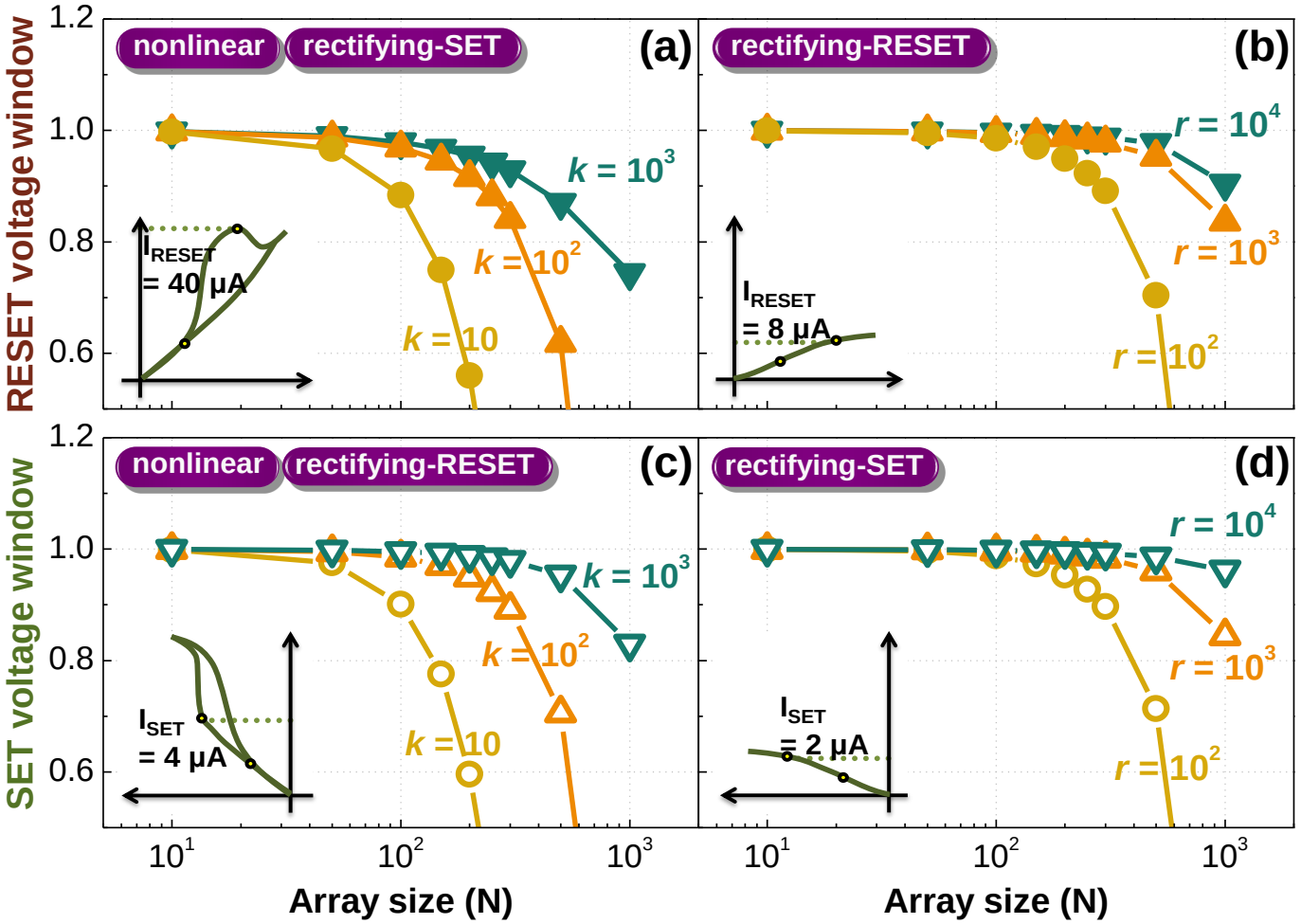
# Selector Analysis During Write

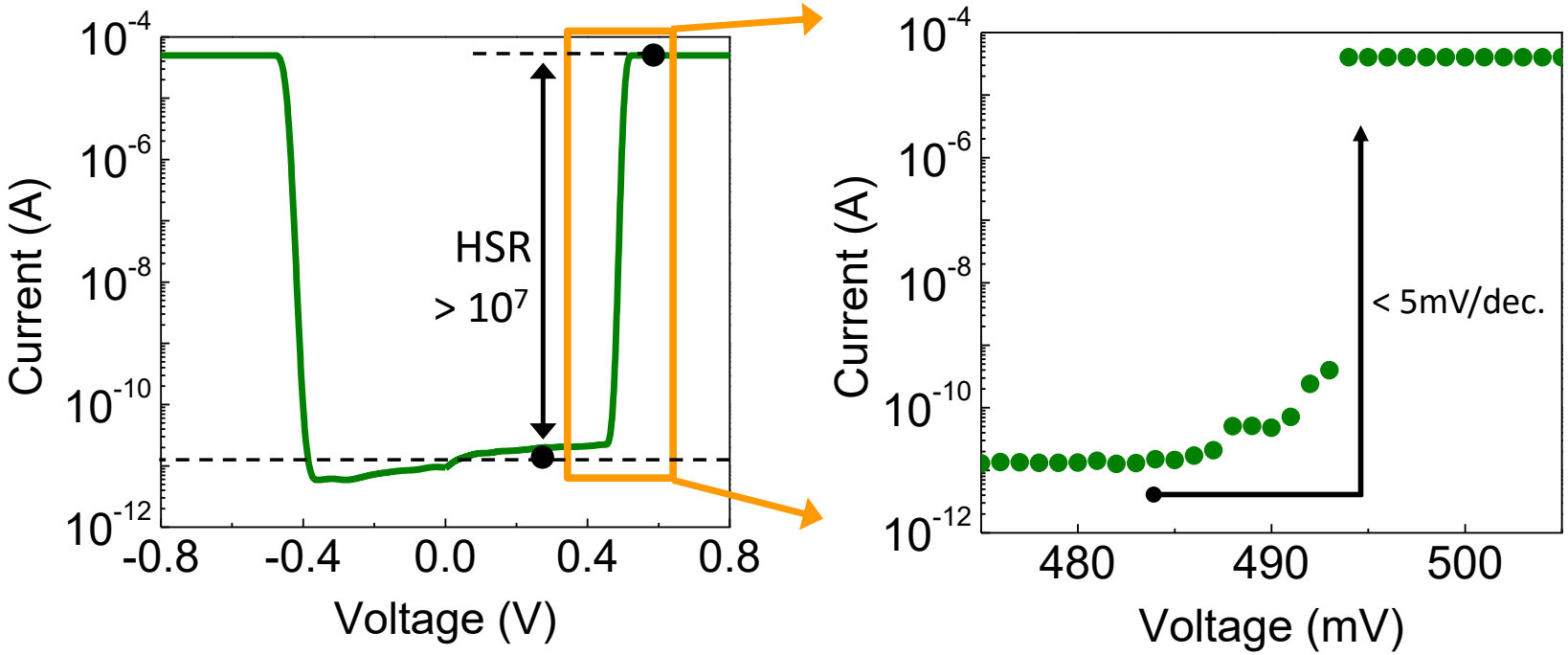



Kim et al. IEEE TED, 61 (8), 2820-2826 (2014).

- Selectivity > 1e5 is desired
- Current density and sub-threshold slope critical

# Selectivity (HSR) & Switching Slope

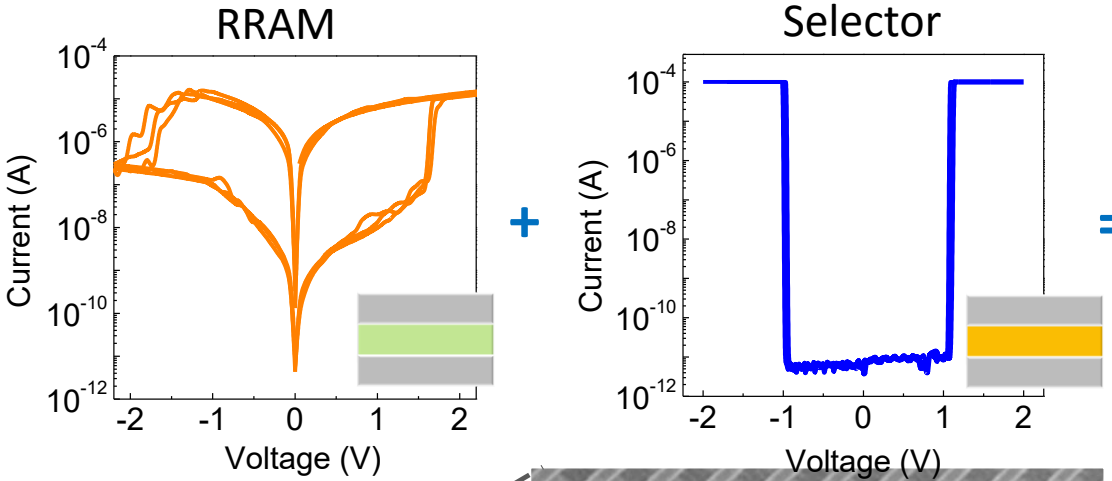
- Half Select Ratio (HSR, $I_{@V}/I_{@0.5V}$) of > $10^7$
  - Enables larger array & reduced power consumption
- Extremely sharp switching of < 5mV/dec.
  - Offers more read voltage margin & faster read

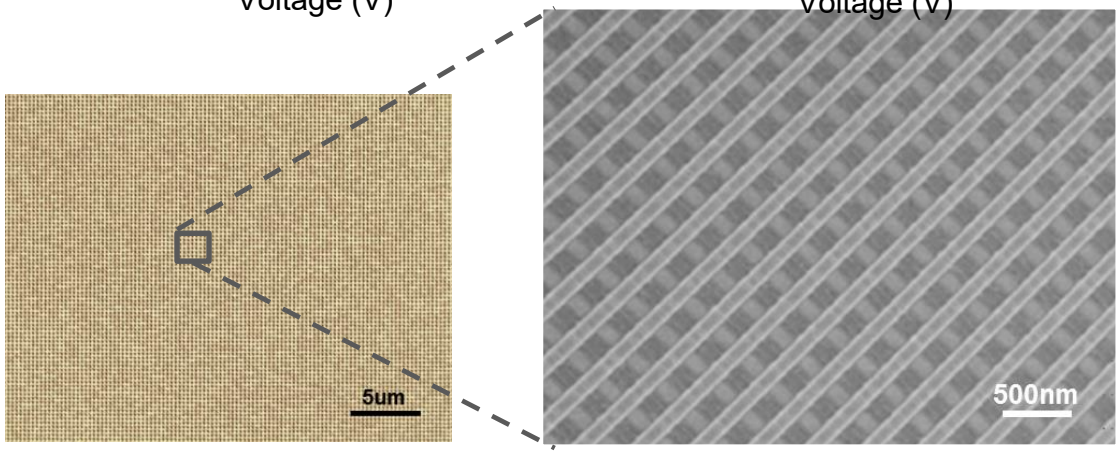



S. H. Jo et al., IEDM 2014

# RRAM + Selector (1S1R) Cell structure

- Cross-point array integration of RRAM + selector
  - High HSR & sharp switching of a selector maintained
  - Small voltage overhead for selector integration



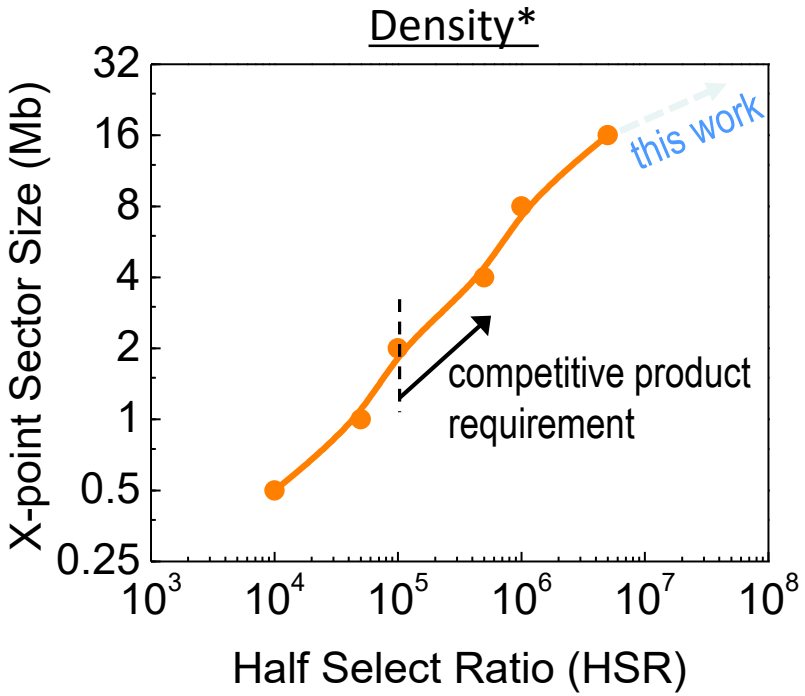



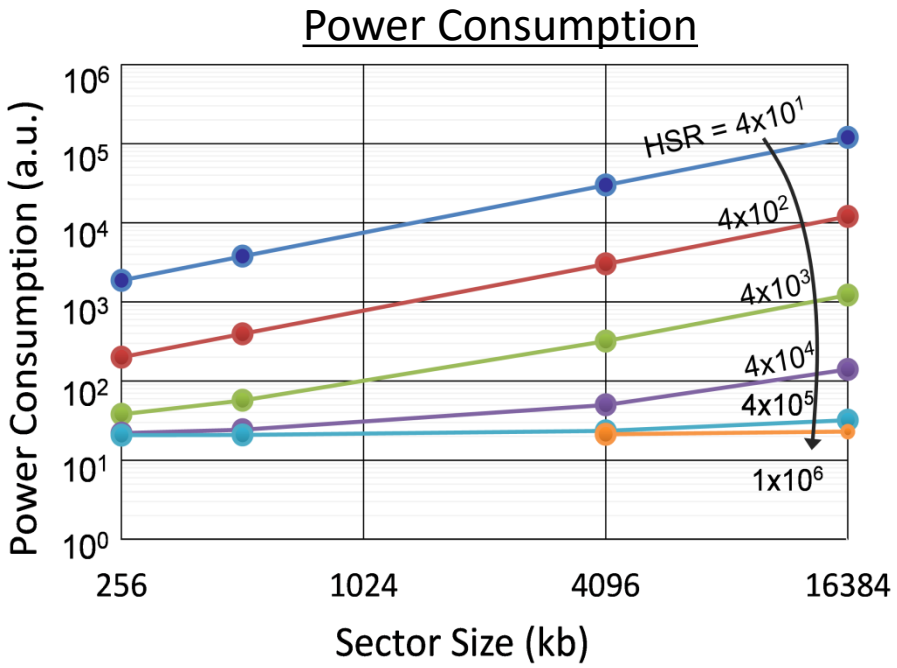

S. H. Jo et al., IEDM 2014

Lu Group
U. Michigan

# Benefits of High HSR

- Large HSR enables high density & low power products



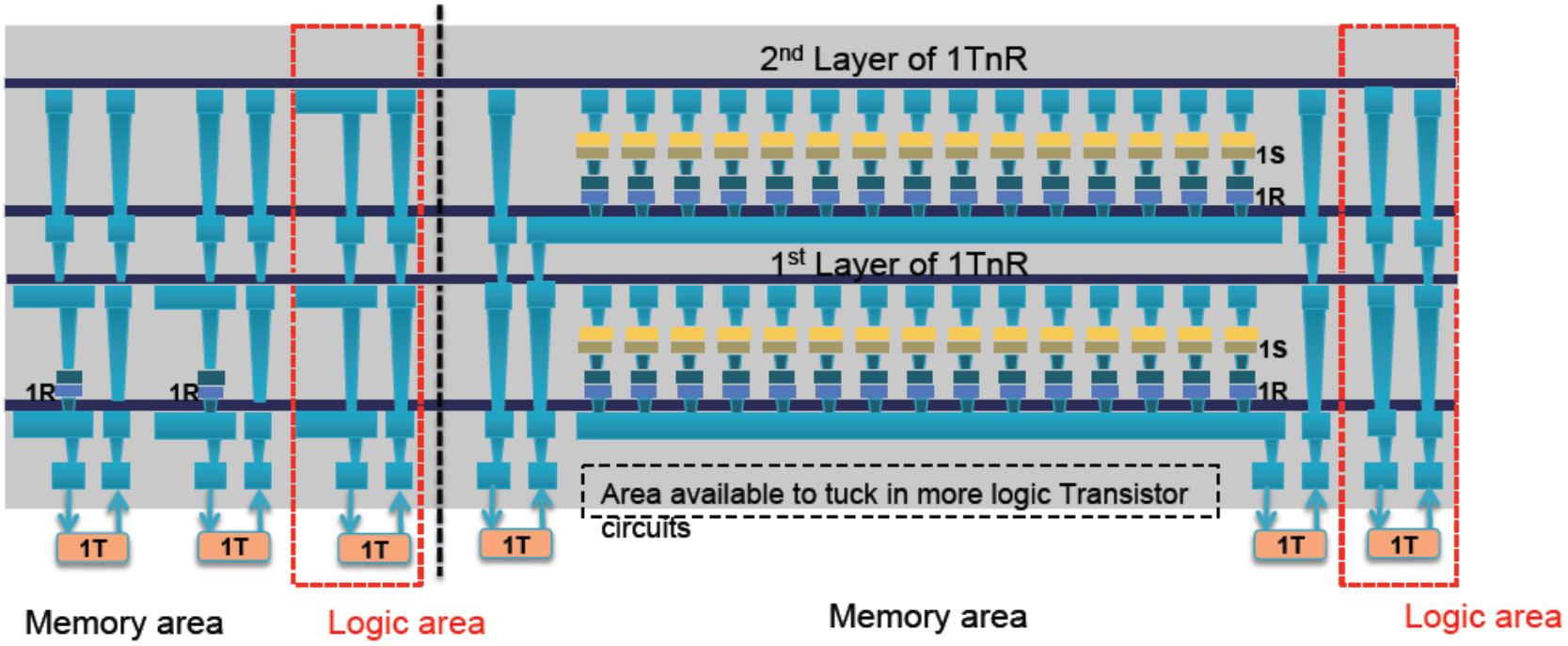




*assumed ICC = 20mA (NAND budget, 2kb cells programmed simultaneously)

S. H. Jo et al., IEDM 2014

# System-Level Innovations

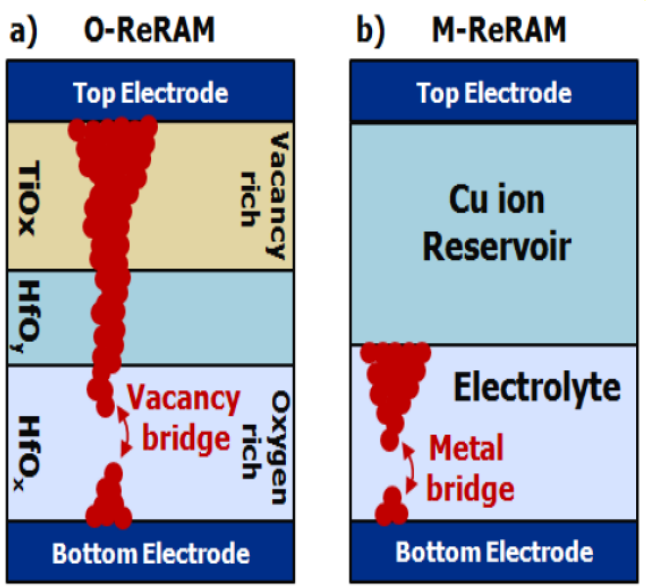
- Code execution and storage class memory on same chip with shared process steps
- Existing tool set in Logic Fabs capable of processing this chip



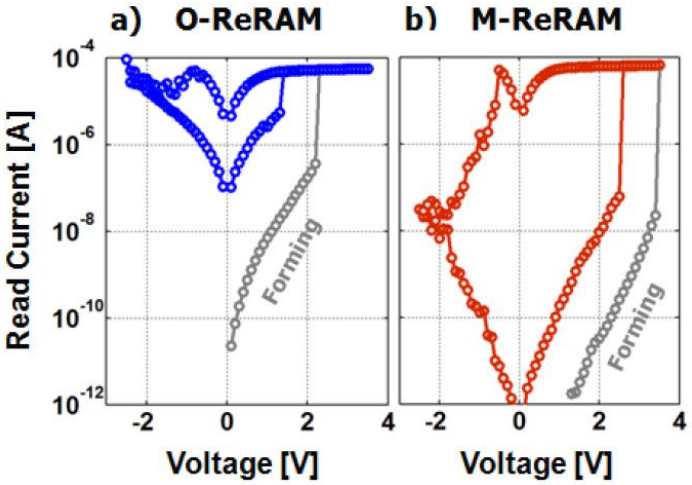
# Comparison of CBRAM and Oxide-RRAM

**CBRAM shows superior performance than oxide-RRAM**

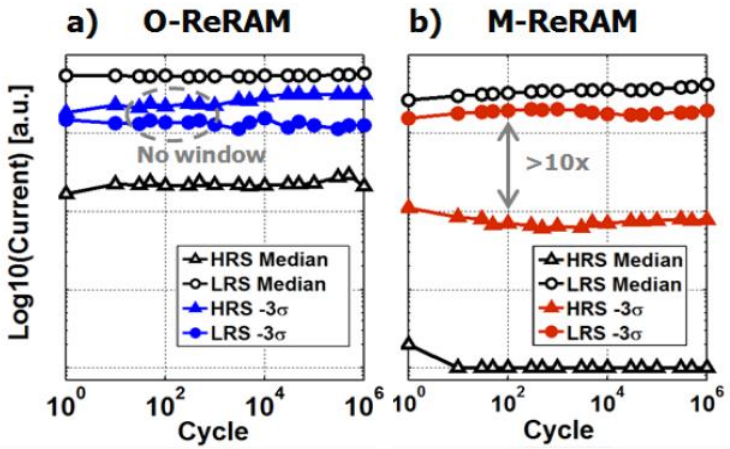
- **Lower variability**
- **Lower BER for cycling and retention due to larger on/off ratio**



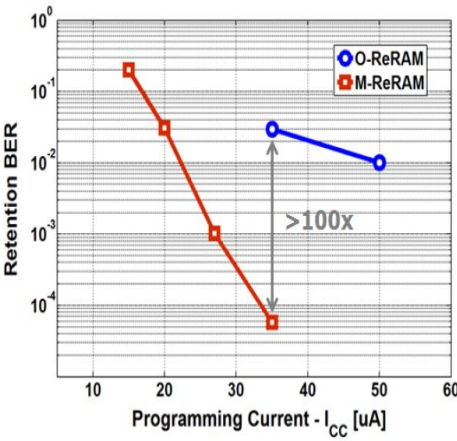

## DC




## Cycling




## Retention




A. Calderoni et al., Micron, IMW 2014

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# Modeling of Oxide RRAM Switching Process

- **Dependent variables**
  - $n_D$ Concentration of $V_o$ [$cm^{-3}$]
  - $T$ Temperature [K]
  - $\psi$ Potential [V]
- **Constants**
  - $a$ Hopping distance, 0.1 nm
  - $f$ Escape-attempt frequency, $10^{12}$ Hz
  - $E_a$ Diffusion barrier, 0.85 eV

- **Oxygen vacancy transport**

Eq.(1) $$\frac{\partial n_D}{\partial t} = \nabla \cdot (D \nabla n_D - v n_D + D S n_D \nabla T)$$

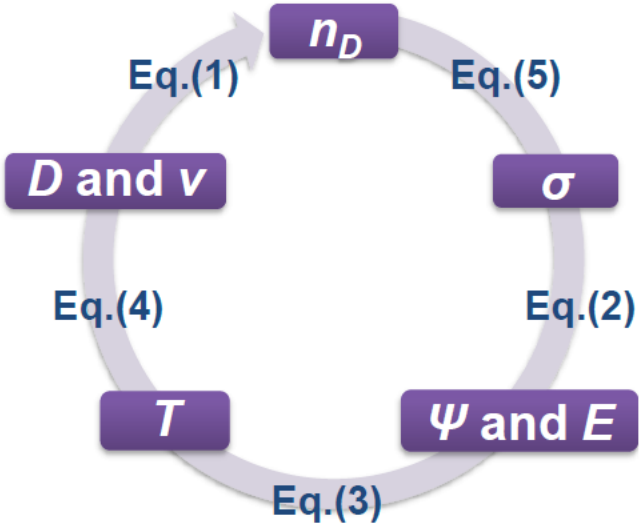
- **Current continuity**

Eq.(2) $$\nabla \cdot \sigma \nabla \psi = 0$$

- **Heat (Joule heating)**

Eq.(3) $$-\nabla \cdot k_{th} \nabla T = J \cdot E = \gamma \cdot \sigma \, | \nabla \psi |^2$$

($\gamma$ = 1 for DC, and $\gamma$ = 2 for AC simulation)




- **Parameters** - Eqs.(4)

$$D = 1/2 \cdot a^2 \cdot f \cdot \exp(-E_a / kT)$$ Diffusivity of $V_o$ [$cm^2 s^{-1}$]

$$v = a \cdot f \cdot \exp(-E_a / kT) \cdot \sinh(qaE / kT)$$ Drift velocity of $V_o$ [cm/s]

$$S = -E_a / kT^2$$ Soret diffusion coefficient [1/K]

S. Kim, S. Choi, W. Lu, ACS Nano, 8, 2369–2376 (2014).

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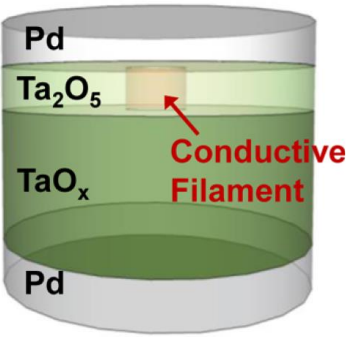
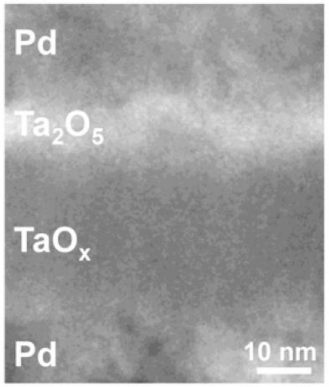
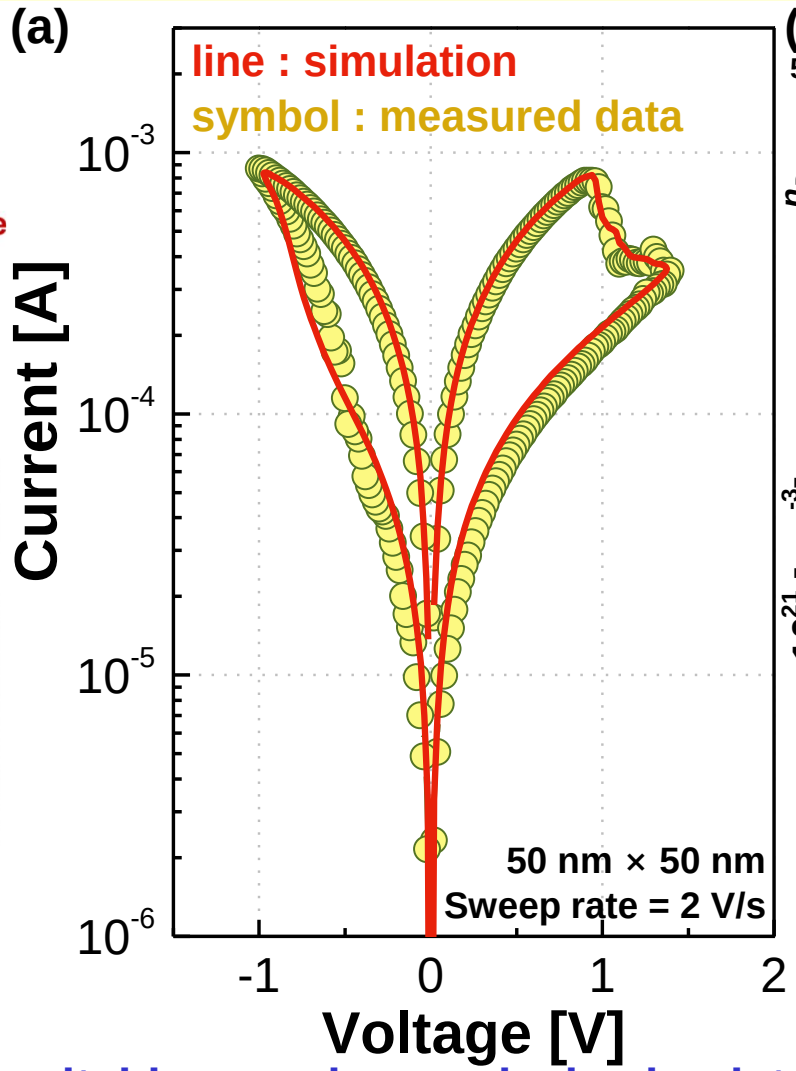
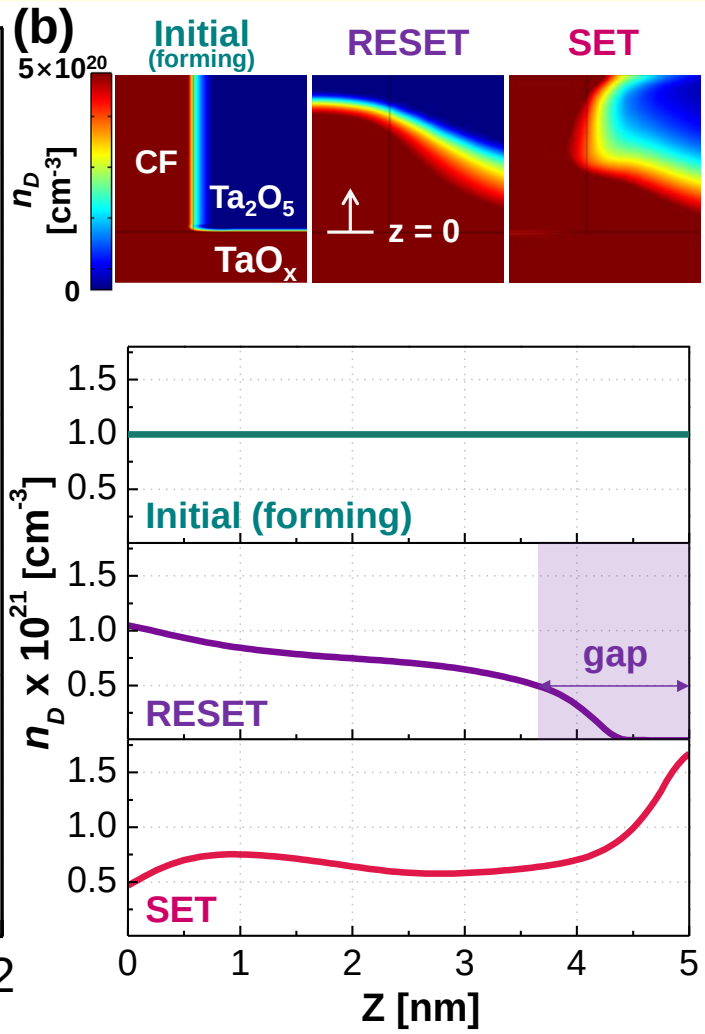
# Oxide-RRAM (Memristor: resistor + memory)



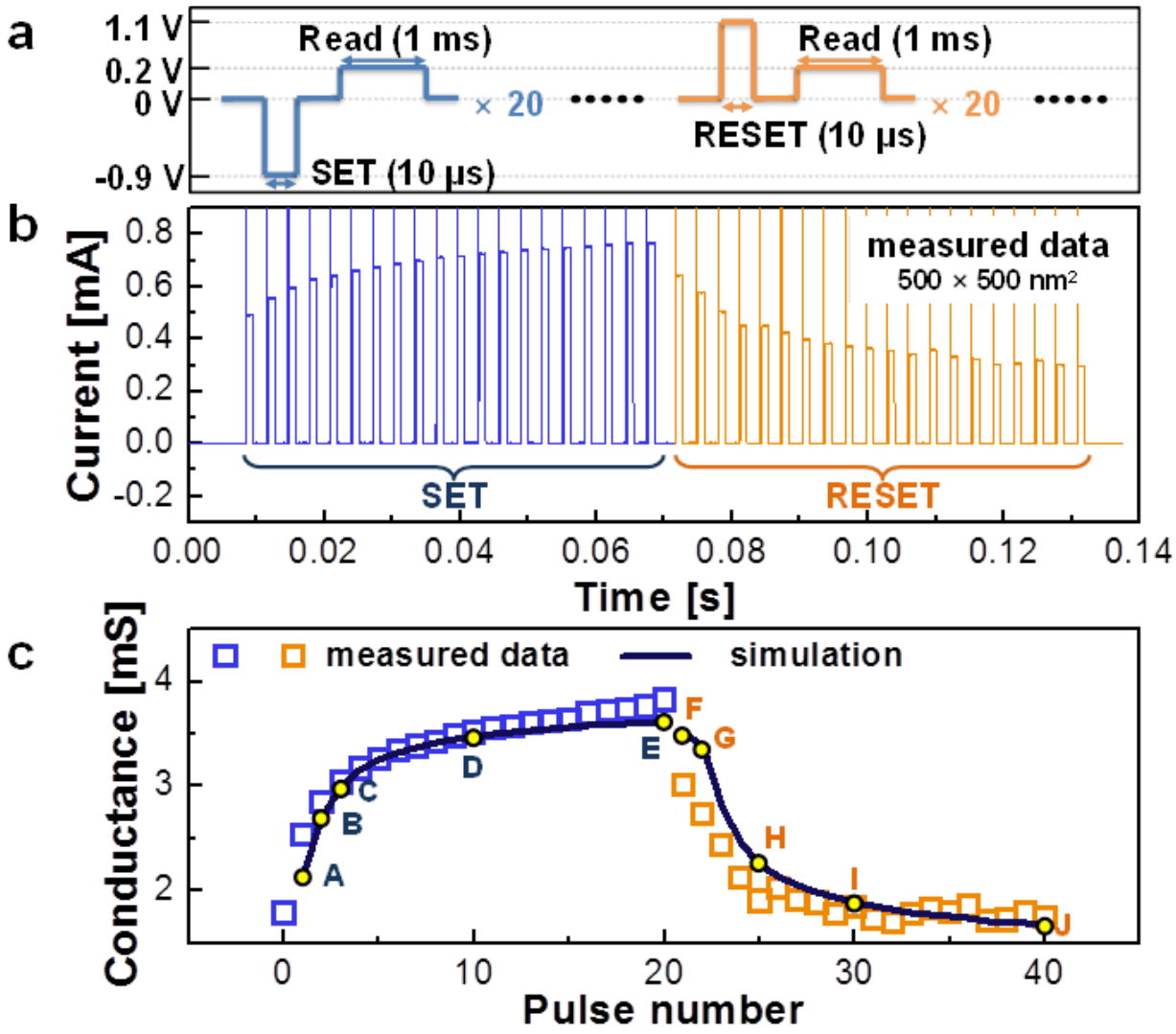




- Resistive switching can be precisely simulated after considering $V_O$ diffusion, drift and thermophoresis effects

S. Kim, S. Choi, W. Lu, ACS Nano, 8, 2369–2376 (2014).

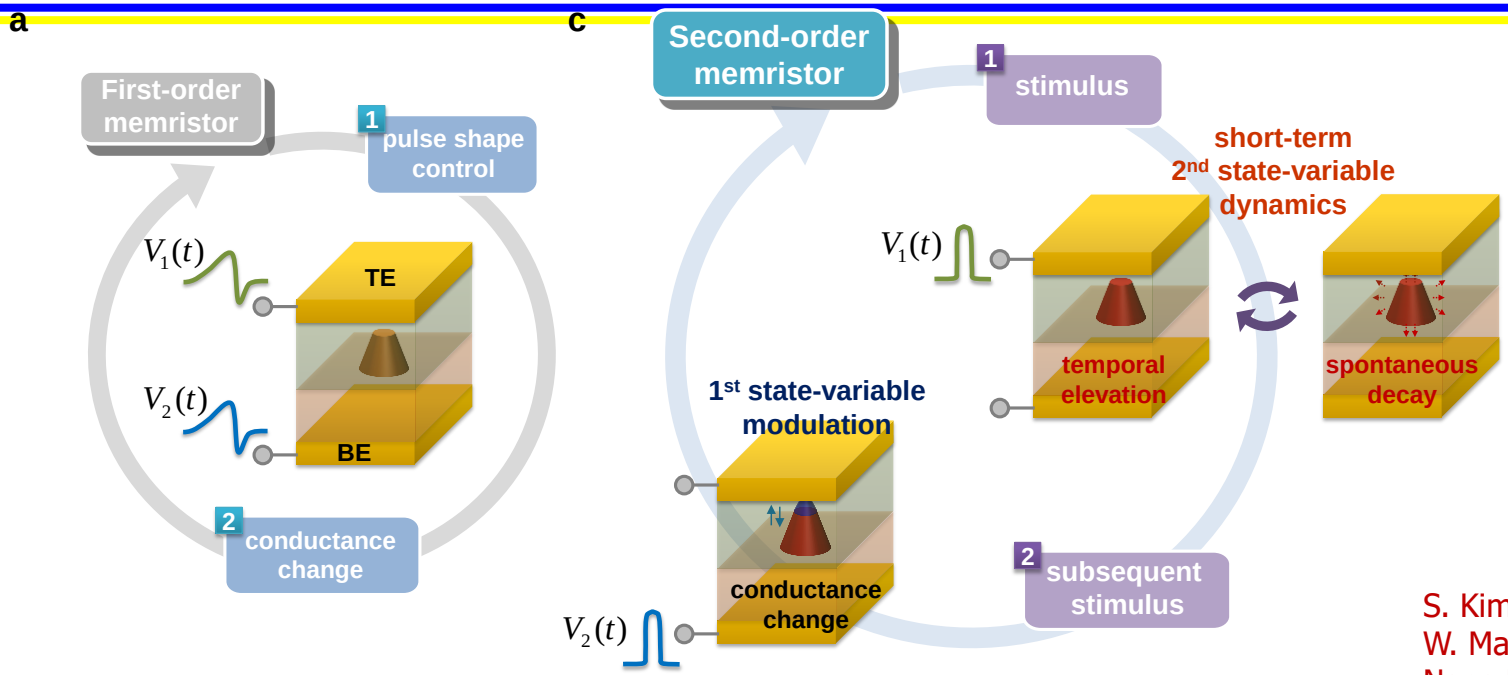
# Simulation of Filament Growth



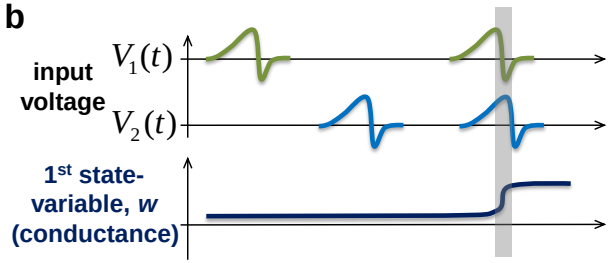

- Same set of parameters can explain both DC and pulse response

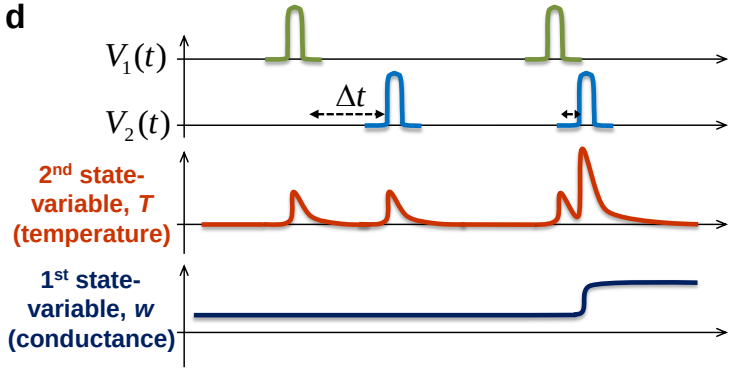
S. Kim, S. Choi, W. Lu, ACS Nano , 8, 2369–2376 (2014)

# Internal Dynamics in a Second-Order Memristor




S. Kim, C. Du, P. Sheridan, W. Ma, S. Choi, W.D. Lu, Nano Lett, **15**, 2203–2211 (2015).




$$\frac{dw}{dt} = f(w,T,V,t)$$

**Weight (conductance) state variable**

$$\frac{dT}{dt} = f(T,V,t)$$

**2nd order state variable that offer (short-term) internal dynamics**

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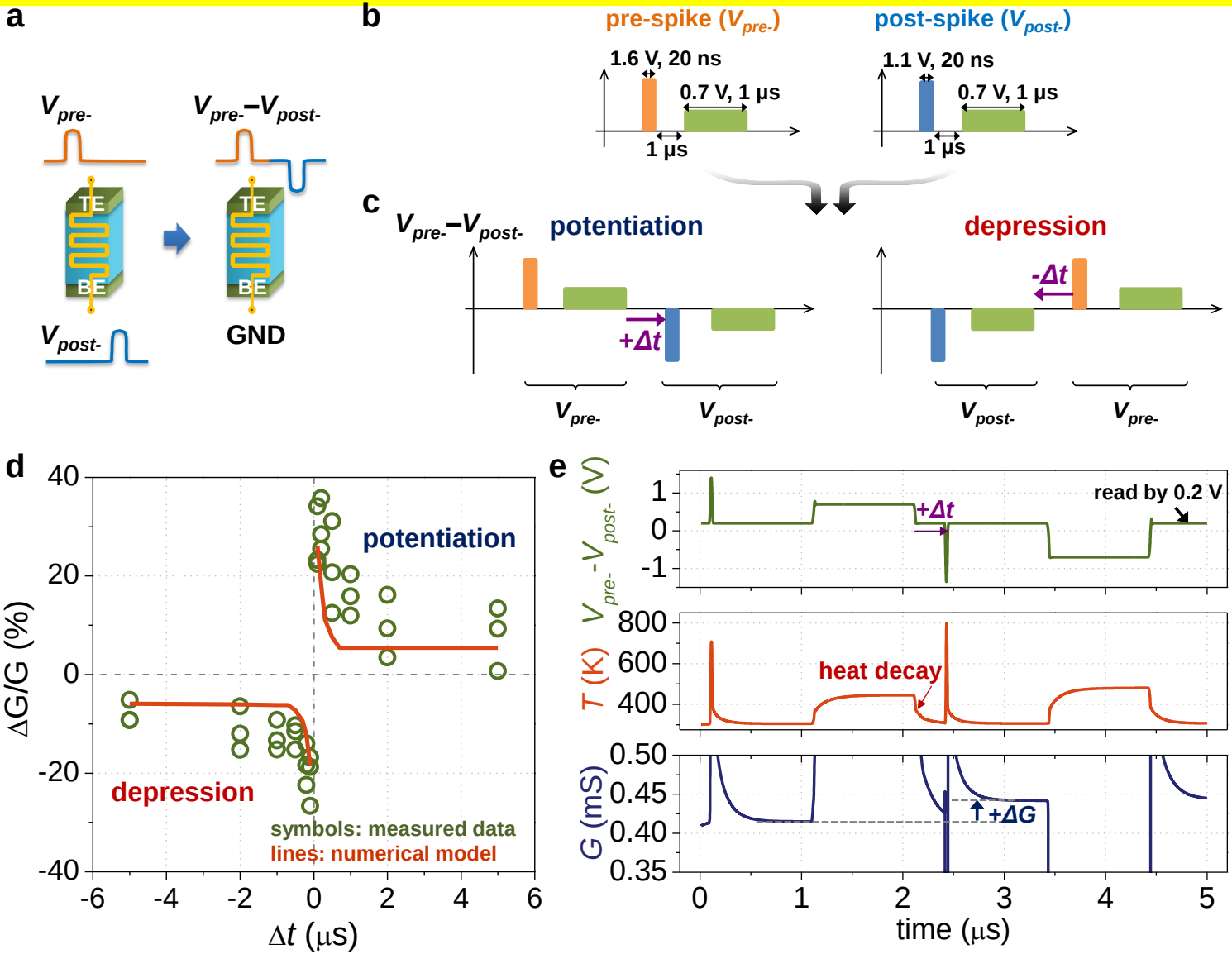
# Implementing STDP (and Spiking Rate Dependent Plasticity) Naturally




S. Kim, C. Du, P. Sheridan, W. Ma, S. Choi, W.D. Lu, Nano Lett, 15, 2203 (2015).

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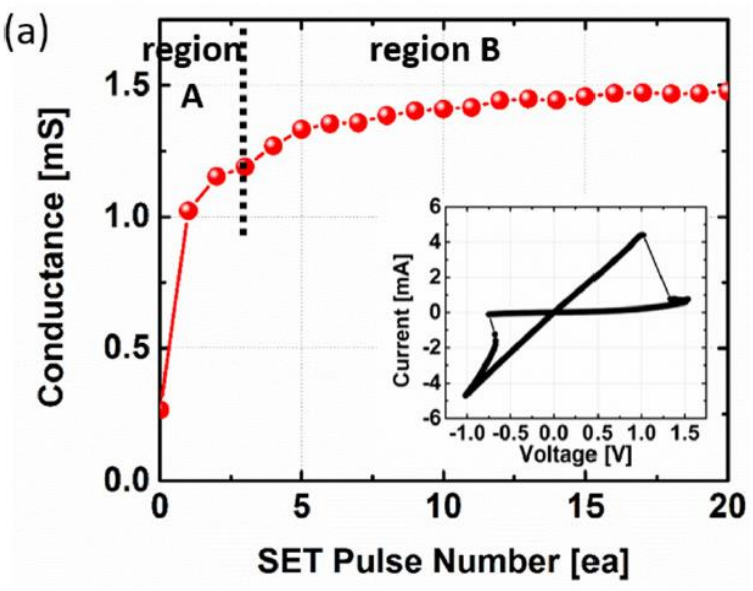
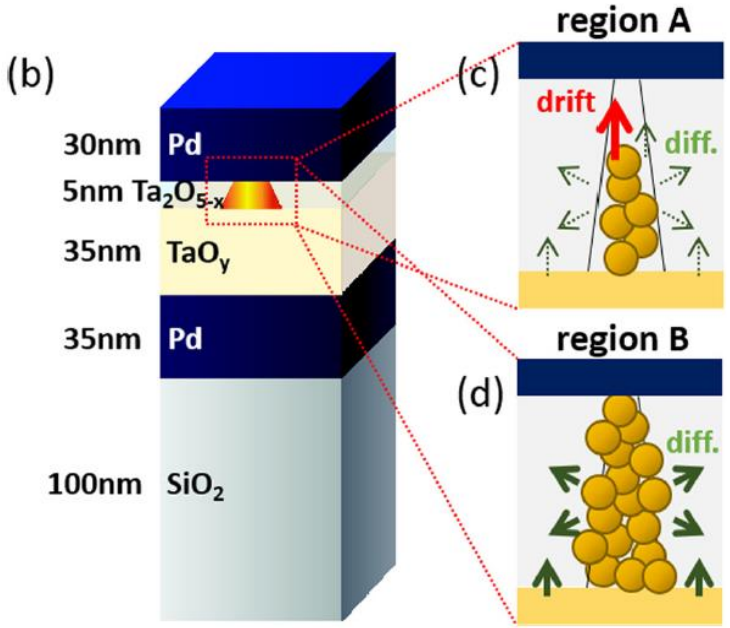
# Improving Analog Switching Using Multiple State Variables

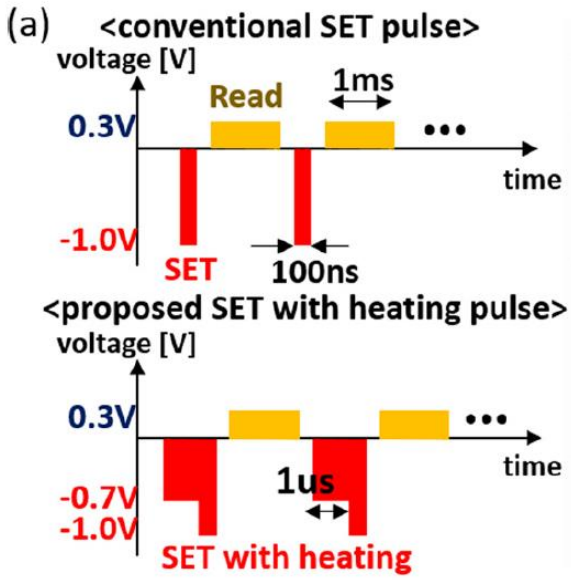


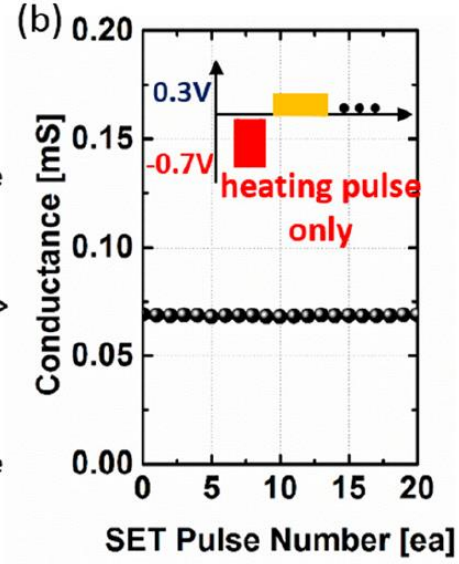



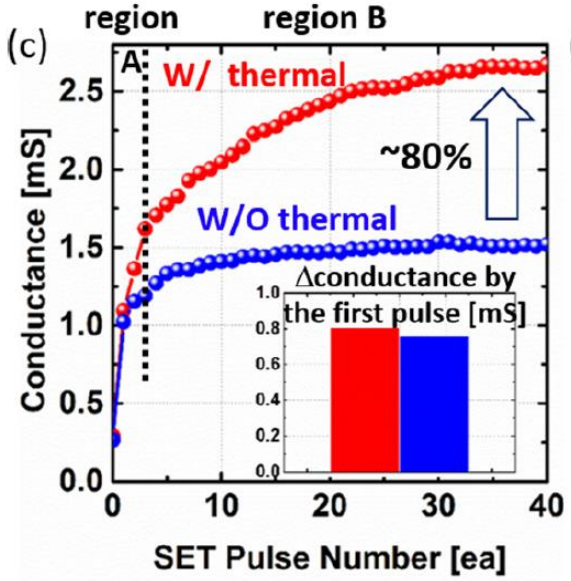

- In oxide RRAM, filament length growth results in gap filling, followed by filament widening
- resistance change due to length growth is non-linear – first few pulses resulting in most resistance change
- More linear response occurs during filament widening, at reduced field
- Needs to selectively enhance the second stage growth (more strongly affected by diffusion)

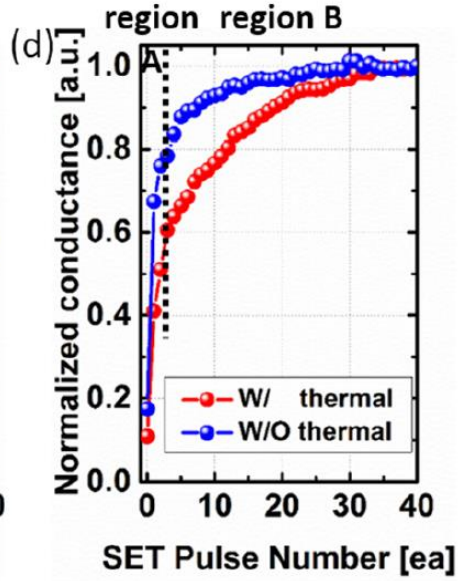
Jeong et al, APL, 107, 173105 (2015)

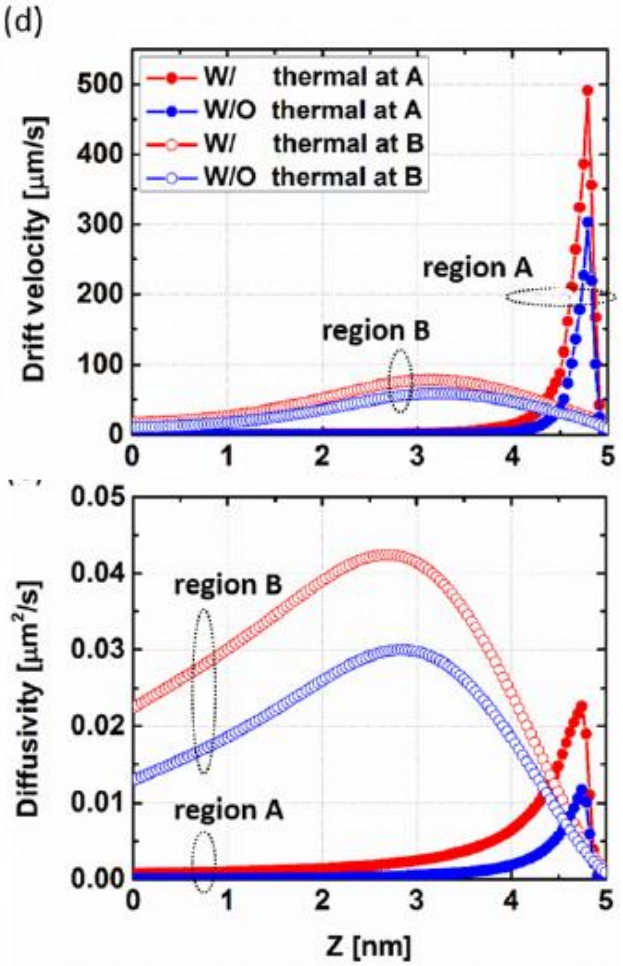
# Improving Analog Switching Using Multiple State Variables




Low amplitude “heating” pulse selectively enhances the filament widening effect, leading more linear pulse response

Jeong, APL, 107, 173105 (2015)

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# Sparse Coding with Memristor Arrays

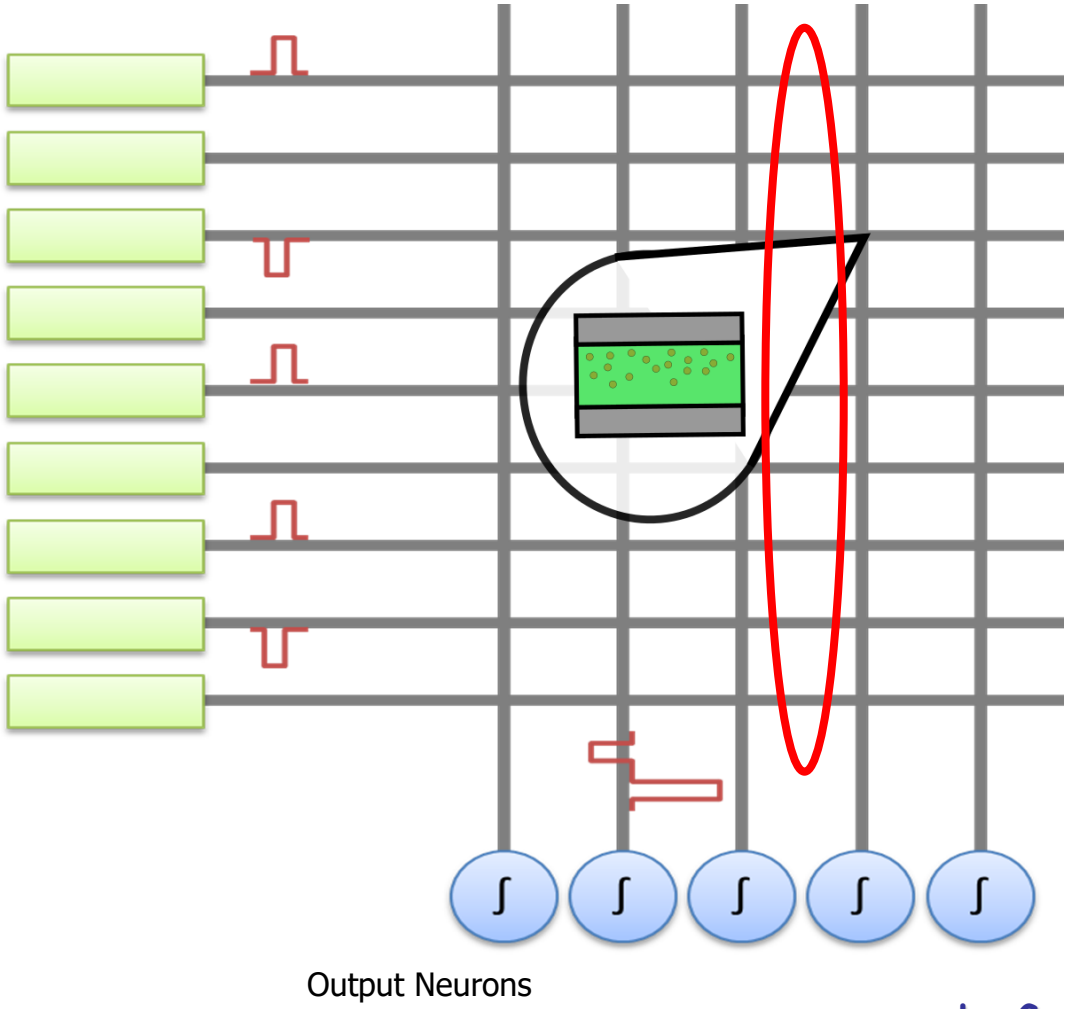
**Memristors perform learning and inference functions**

DARPA UPSIDE program

- Memristor weights form dictionary elements (features)
- Image input, Pixel intensity represented by # of pulses
- Memristor array natively performs matrix operation

$$\vec{I} = \vec{v} \cdot \overleftrightarrow{\Phi}$$

- Integrate and fire neurons
- Learning achieved by backpropagating spikes



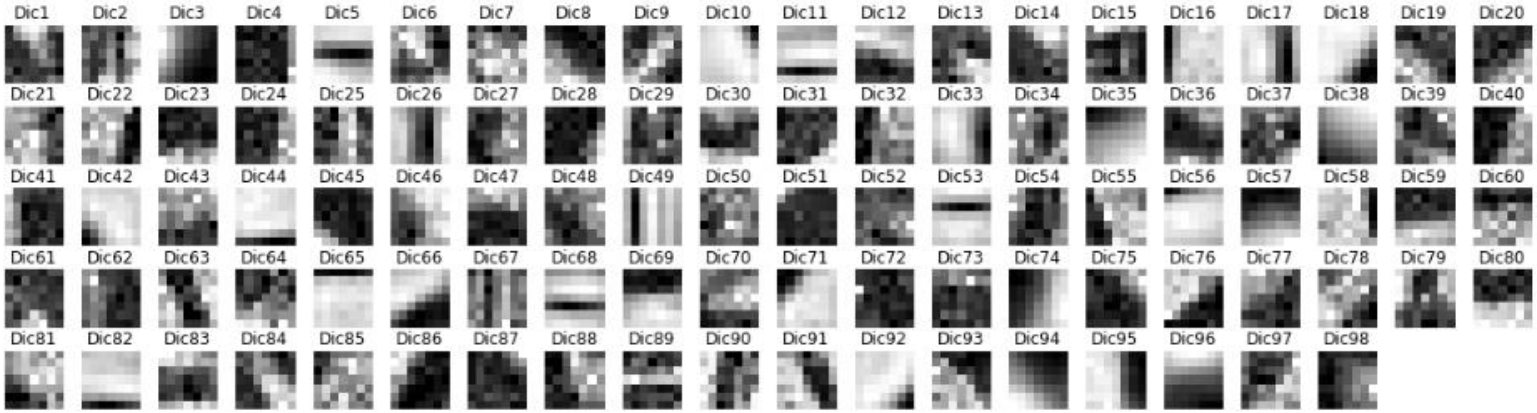
# Image Reconstruction with larger 7x7 patches (48x98 memristor array)

**Original**

**Software reconstruction**

**Crossbar with variations**

**Learned receptive fields**



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**Dr. Sungho Kim*
*Dr. Bing Chen*
**Dr. Taeho Moon*
**Dr. Zhongqing Ji*
** Dr. Qing Wan*

## Visiting scholars:

*Dr. L. Liu*
**Xiaojie Hao*

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- Dr. G. Kenyon, LANL
- Prof. C. Teuscher, PSU
- Prof. D. Strukov, UCSB,
- Prof. J. Hasler, GeorgiaTech,
- Prof. R. Li, CAS, China
- Dr. I. Valov, Prof. R. Waser

Crossbar

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* alumni

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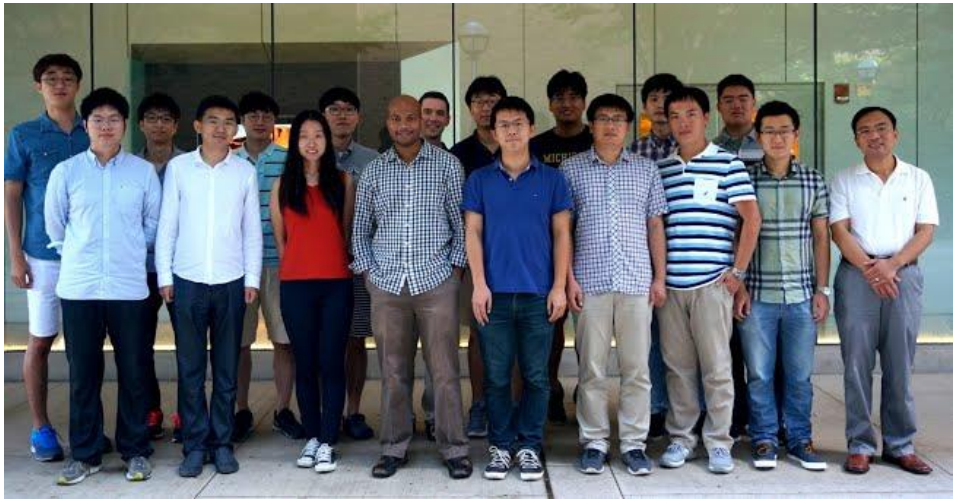

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